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UNIVERSITY TEKNOLOGI PETRONAS

RECONFIGURABLE POWER AMPLIFIER WITH TUNABLE INTERSTAGE MATCHING NETWORK USING GaAs MMIC AND SURFACE-MOUNT TECHNOLOGY

by

Regina Gani

The undersigned certify that they have read, and recommend to the Postgraduate Studies Programme for acceptance this thesis for the fulfillment of the requirements for the degree stated.

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RECONFIGURABLE POWER AMPLIFIER WITH TUNABLE INTERSTAGE MATCHING NETWORK USING GaAs MMIC AND SURFACE-MOUNT TECHNOLOGY

by

Regina Gani

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Title of thesis: RECONFIGURABLE POWER AMPLIFIER WITH TUNABLE INTERSTAGE MATCHING NETWORK USING GaAs MMIC AND SURFACE-MOUNT TECHNOLOGY

I REGINA GANI

hereby declare that the thesis is based on my original work except for quotations and citations which have been duly acknowledged. I also declare that it has not been previously or concurrently submitted for any other degree at UTP or other institutions.

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To Barry.

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ABSTRACT

As the demand of reconfigurable devices increases, the possibility of exploiting the interstage matching network in a two-stage amplifier to provide center frequency tuning capability is explored. While placement of tuning elements at the input and/or output matching network has some disadvantages, placement of tuning elements in the interstage absorbs the lossy components characteristics into useful attributes. The circuit design methodology includes graphical method to determine the bandpass topology that achieves high Q-contour on the Smith chart thus result in narrow bandwidth. T-section and π-section topologies are used to match reactive terminations provided by the first and second amplifier stages. The design methodology also includes utilization of interstage mismatch loss that decreases as increasing frequency to compensate for amplifier gain roll-off and equalize the gain at different tuning states.

In prototype realization, three design configurations are discussed in this thesis: 1) a discrete design for operation between 0.1 – 0.9 GHz with the total layout area of 7.5 mm x 12.5 mm, 2) a partial monolithic design (Quasi-MMIC) for operation between 0.9 – 2.4 GHz that is 25 times smaller layout area compared to the discrete design, and 3) a conceptual design of integrated monolithic reconfigurable PA for operation between 0.9 – 2.4 GHz that is 130 times smaller layout area compared to the discrete design. One variant of the fabricated reconfigurable PA offers advantage of 4-states center frequency tuning from 1.37 GHz to 1.95 GHz with gain of 21.5 dB ($\pm$ 0.7 dB).

The feasibility of interstage matching network as tuning elements in reconfigurable power amplifier has been explored. The input and output matching networks are fixed while the interstage impedances are varied using electronic switching (discrete SP4T and GaAs FET switches). The discrete design is suited for

the operation at low frequency (f_o < 1GHz), while monolithic implementation of the tunable interstage matching network is required for higher frequency operation due to size limitation and parasitic effects. The reconfigurable PA using MMIC tuner was designed at higher frequency to possibly cover GSM, CDMA, Bluetooth, and WiMAX frequency (0.9 – 2.4 GHz).

ABSTRAK

Dengan peningkatan permintaan alat-alat *reconfigurable*, kemungkinan memanfaatkan *interstage matching network* untuk menyediakan kemampuan *tuning* frekuensi tengah telah dieksplorasi. Penempatan elemen *tuning* pada bahagian *input* dan/atau *output* mempunyai beberapa kelemahan sedangkan penempatan elemen *tuning* di bahagian *interstage* dapat menyerap karakteristik elemen *lossy* menjadi atribut yang berguna. Metodologi desain litar termasuk kaedah grafik untuk menentukan topologi yang mencapai Q-kontur yang tinggi pada *Smith chart* sehingga mencapai *bandwidth* yang sempit. Topologi *T-section* dan *π-section* digunakan untuk menyesuaikan impedansi reaktif yang disediakan oleh penguat tahap pertama dan kedua. Metodologi desain juga meliputi pemanfaatan *interstage mismatch loss* untuk mengkompensasi *gain roll-off* penguat dan menyamakan *gain* pada frekuensi yang berbeza.

Dalam merealisasikan prototaip, tiga konfigurasi desain dibahas dalam tesis ini: 1) desain *discrete* untuk operasi antara 0.1 – 0.9 GHz, 2) rancangan monolitik separa untuk operasi antara 0.9 – 2.4 GHz yang 25 kali lebih kecil dibanding dengan *layout* desain *discrete*, dan 3) desain konseptual monolitik *reconfigurable PA* yang bersepadu untuk operasi antara 0.9 – 2.4 GHz yang 130 kali lebih kecil dibanding dengan *layout* desain *discrete*. Salah satu variasi *reconfigurable PA* menawarkan kelebihan iaitu tuning empat *state* frekuensi dari 1.37 GHz hingga 1.95 GHz dengan *gain* 21.5 dB ($\pm$ 0.7 dB).

Kelayakan *interstage matching network* sebagai elemen *tuning* untuk *reconfigurable power amplifier* telah dieksplorasi. *Matching network* pada bahagian *input* dan *output* adalah tetap, sedangkan impedansi *interstage* bervariasi dengan menggunakan *switching* elektronik (SP4T dan GaAs FET switch).Desain *discrete* sesuai untuk operasi pada frekuensi rendah (f_o < 1GHz), sedangkan pelaksanaan

monolitik dari *tunable interstage matching network* diperlukan untuk operasi frekuensi yang lebih tinggi kerana batasan ukuran dan kesan parasit. *Reconfigurable PA* yang menggunakan *tuner MMIC* direka pada frekuensi yang lebih tinggi untuk melingkupi operasi frekuensi GSM, CDMA, Bluetooth, dan frekuensi WiMAX (0.9 – 2.4 GHz).

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

LIST OF ABBREVIATIONS

ADS	Advanced Design Systems
BPF	Band Pass Filter
BW	Bandwidth
COTS	Commercially Off-The-Shelf
CPW	Co-Planar Waveguide
dB	decibel
DRC	Design Rule Check
DUT	Device under Testing
EM	Electro-Magnetic
GaAs	Gallium Arsenide
GPS	Global Positioning System
HBT	Heterojunction Bipolar Transistor
IL	Insertion Loss
InGaP	Indium Gallium Phosphor
LO	Local Oscillator
LVS	Layout versus Schematic
MESFET	Metal Semiconductor Field Effect Transistor
MEMS	Micro Electro-Mechanical Systems
MIM	Metal-Insulator-Metal
MMIC	Monolithic Microwave Integrated Circuits
MN	Matching Network
NA	Network Analyzer
OIP3	3^{rd} Order Intercept Point
P_{1dB}	1dB-Gain Compression
PA	Power Amplifier
PAE	Power Added Efficiency
PCB	Printed Circuit Board

pHEMT	psudomorphic High Electron Mobility Transistor
PTH	Plated-Through Hole
RL	Return Loss
SDR	Software-Defined Radio
SMA	Surface-Mount Assembly
SMD	Surface-Mount Devices
SMT	Surface-Mount Technology
SP4T	Single Pole 4 Throw
SPDT	Single Pole Double Throw
TOI	Third Order Intercept

CHAPTER 1

INTRODUCTION

Today, modern mobile phones are not only devices used for communication, they are also a part of our lifestyle. Voice and video call, text and multimedia messaging with fast data transfer, Wi-Fi capability, GPS navigation and mobile TV are some of the supported features offered by the new high-end mobile devices. As the demand of new applications rise, engineers are competing to search ways to support the numerous standards without degrading system performance, but even improving it.

Chapter 1 provides an introduction to the research background, problem statements, objectives and the chapter organization.

1.1 Background Study

In the last 50 years, wireless communications industry experienced dramatic changes driven by many technology innovations. This has led to numerous standards for wireless communication. Some of the commercially available standards are the analog and digital cellular telephony (CDMA, GSM, TDMA, UMTS, TETRA), networking (802.11 family, Bluetooth, WiMAX, ZigBee) and many more. Most of these standards occupy the frequency in L band (1 – 2 GHz) and S band (2 – 4 GHz). As mentioned in [1] – [4], the incompatibility between standards due to development in different continent (Europe, Japan and USA) increases the need for a reconfigurable mobile system.

There are several types of RF front-end architecture that precede any communication system standard: heterodyne receiver, homodyne receiver and low IF receiver. A method to enable reconfigurability at the RF front-end could be a simple switchable system where a “cold switch” is used to choose which standard is

working without affecting the other standards. Another method is to reuse common function blocks to fulfill the requirements of both standards. The more advanced method is to build multifunctional building blocks that provide a merged architecture of some standards [4].

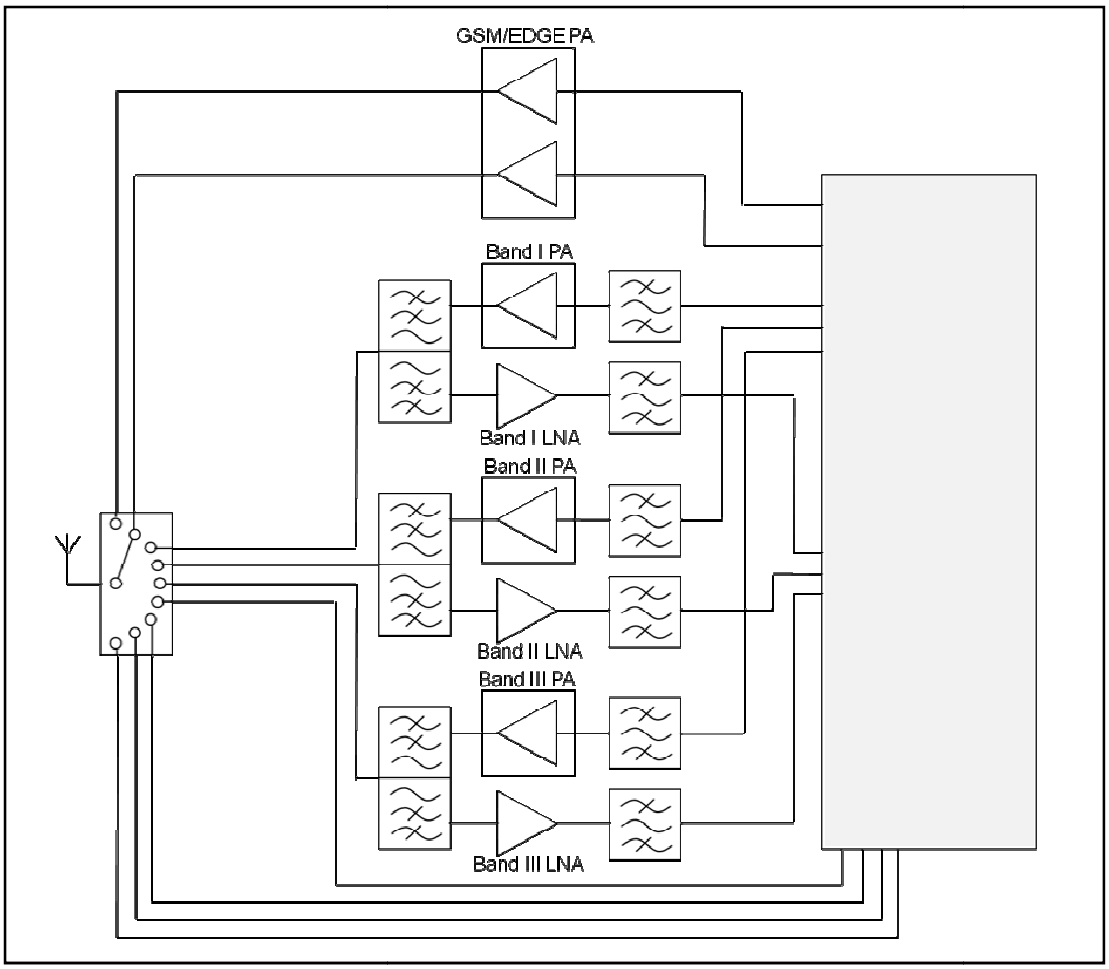


Figure 1.1 Traditional RF front end to support multiple standards [5]

Traditional ways to support multiple air interface standards is by having stacked radio architecture with separate radio transceivers for different standards as shown in Figure 1.1. This approach is not practical for multiband mobile device because the duplication of functions yield in high power consumption, large product size and cost increment [5]. Other performance degradations occur because of the unwanted interaction between the function blocks.

The path towards modern technology shows that multifunction and reconfigurable capabilities must be incorporated into mobile wireless system

technology [2] – [3]. It is evident that the effort towards multifunctional RF system requires development of tunable or switchable and reusable RF components.

1.2 Problem Statement

Modern technologies are focusing on multifunctional RF system where reuse of components is maximized, integration of RF functions is preferable and simultaneous tasks are performed. One of the interests in multifunctional RF systems is switchable and tunable components [2].

The challenges faced by the RF front-end in wireless mobile communications include handling multiple carrier frequencies, widely varying RF power levels, differing modulation formats, linearity specifications and varying impedances provided by the antenna. According to [4] and [6] – [8], the approaches used to meet these challenges are adaptive power amplifiers that have the capability of reconfiguring their characteristics to meet varying specifications.

The common approach to operate power amplifier in multiple bands is to switch between several amplifiers. However, this type of multiband power amplifier is complex, bulky, expensive and occupies large area [9] – [10]. Another approach is to use wideband amplifiers that cover a wide range of frequencies. Power amplifier is the device that consumes the most amount of power in the RF front-end. Therefore, power amplifiers must operate at high efficiency. However, it is difficult for wideband power amplifiers to operate with adequate performance (gain, efficiency, power consumption, etc) in comparison with the single band power amplifier [4], [9] – [12].

There are several characteristics of amplifiers that require adaptive functions, such as: variable output frequency, variable output power, variable modulation format, variable antenna impedances and variable interference sources and constraints [4]. According to reference [4]:

"It is highly desirable to have power amplifiers that can operate on any chosen frequency band. However, as dictated by Fano's Theorem, the performance

metrics of an amplifier are invariably better over a narrow band than over a wide bandwidth" (Steer, 2008).

In current broadband RF systems, filtering dominates size and cost [1], [4]. Most of the filters are not tunable and hence limit the usable frequency range of most RF front ends. An alternative to the use of static filters before or after power amplifier is reconfigurable power amplifier which can be difficult to design for high performance. Power amplifier is a significant device whose existence is unavoidable in RF front-end architecture. Therefore, this work proposes a development of reconfigurable power amplifier with center frequency tuning capability.

Power amplifiers typically consist of input matching network, more than one amplification stage with associated interstage matching and output matching network. Several tunable power amplifiers have been reported in [6], [9], and [12] – [18]. Most of these works obtain the frequency tunability by varying the input and/or output matching network. Utilization of interstage matching network as tuning element has not been extensively exploited. While placing switchable tuning elements in the input side may cause poor noise figure and excessive bandwidth and placement in the output side may results in lower efficiency and output power. Placement of variable tuning elements in the interstage offers several advantages, such as improvement in stability and minimum effect of inductor loss to the gain and bandwidth. Thus, this work focuses mainly in the exploitation of interstage matching networks for power amplifier reconfigurability.

In the development of reconfigurable devices, the primary issues for the design are excessively wide bandwidth and gain fluctuation [19]. This work includes the design methodologies used to achieve reconfigurable power amplifier with narrow bandwidth and the technique to utilize interstage mismatch loss for gain equalization. In the prototype realization, two different circuit configurations were used: 1) surface-mount components and 2) GaAs Monolithic Microwave Circuit.

1.3 Objectives

The motivation for this research is to develop a reconfigurable power amplifier with tunable interstage matching network. The followings are the main objectives of this research:

1. To develop circuit design methodology for reconfigurable power amplifier using tunable interstage matching network that utilizes the lossy component characteristics into useful attributes.
2. To design, fabricate and measure the performance of reconfigurable power amplifier by integrating tunable interstage matching network using Surface-Mount technology with the two-stage MMIC power amplifier (Discrete Design).
3. To design, fabricate and measure the performance of reconfigurable power amplifier by integrating tunable interstage matching network using Gallium Arsenide Monolithic Microwave Integrated Circuits (GaAs MMIC) technology with the MMIC two-stage power amplifier (Quasi-MMIC Design).
4. To design and layout reconfigurable power amplifier by integrating tunable interstage matching network within an integrated GaAs MMIC die (Integrated Design).

1.4 Scope of Study

The scope of this work is listed as follows:

1. The device models used for MMIC interstage matching network design and integrated MMIC design are WIN PD50-01 and WIN PD50-10 0.5μm GaAs E/D-mode pHEMT.
2. The two-stage power amplifier (Amp_A and Amp_B) are available in die form and fabricated using H02U-41 InGaP/GaAs HBT and 0.5μm GaAs pHEMT technology, respectively.

3. Agilent's Advanced Design System (ADS) is used for circuit simulation and layout design.

1.5 Chapter Organization

The report is organized into 6 chapters: 1) Introduction, 2) Literature Review, 3) Methodology, 4) Results and Discussion, 5) Proposed Integrated Reconfigurable GaAs MMIC Power Amplifier Design, and 6) Conclusion.

The first chapter briefly discusses the motivation and objectives of this research work. The second chapter discusses the study and the development trend of adaptive or reconfigurable microwave circuits and systems. The third chapter elaborates the design methodology, experimental setup, fabrication, measurement, and the two main design configurations. Simulated and measured results are discussed and analyzed in Chapter 4. Chapter 5 is dedicated for the proposed integrated MMIC reconfigurable power amplifier design. Finally, chapter 6 concludes the overall work done and provides recommendations for future work.

CHAPTER 2

LITERATURE REVIEW

This chapter discusses the study and the development trend of adaptive or reconfigurable microwave circuits and systems.

2.1 RF Front End

The RF front end is a critical part of a radio that transforms analogue RF signals to digital baseband signals and vice versa. The trade-off between overall system performance, power consumption and size are determined between the receiver front end and the analogue-to-digital converters in the base band [20].

The transceiver, a short term for transmitter-receiver, is a device that both transmits and receives analog or digital signals. RF front end is a generic definition of every system blocks located between the antenna and digital baseband system [21] – [22].

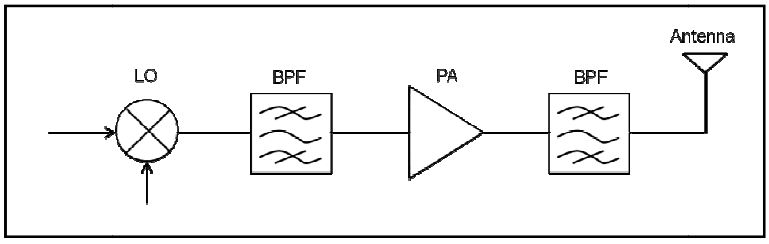


Figure 2.1 Simplified Diagram of Transmitter

Typical goals for the transmitter design include: 1) obtain required output power, 2) maximize linearity, 3) optimize Power Added Efficiency (PAE), and 4) filter unwanted spurious outputs [23]. The transmitters work by up-converting

information, amplify it and transmit the signal as illustrated in the simplified diagram in Figure 2.1.

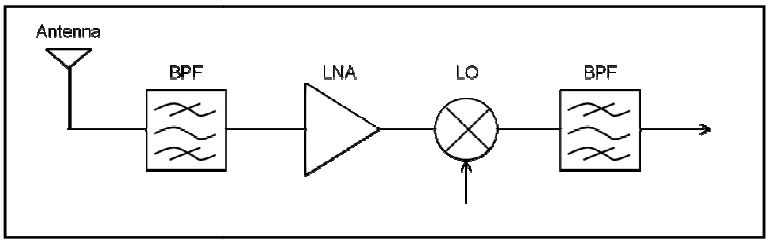


Figure 2.2 Simplified Diagram of Receiver

Typical goals for the receiver design are: 1) to achieve the required sensitivity, 2) to reject spurious products, and 3) to maintain linearity at low supply voltage and current [23]. At the receiver end, the antenna receives modulated RF signals from the RF transmitter which are then amplified by low noise amplifier (LNA) and down-converted to baseband signal. Figure 2.2 shows a simplified diagram of a receiver.

Despite the complicated circuitry, the three main functions of a transceiver can be categorized as filtering, amplification and demodulation.

2.1.1 Filter

The filtering process rejects unwanted signals and passes the desired signals. The filter performance controls the selectivity of receiver detector. Selectivity is a measure of the detector's capability to differentiate signals between adjacent frequency bands.

Filter selectivity is closely related to Q-factor of the bandpass filter. Higher Q-factor corresponds to a narrower bandwidth and faster roll-off which means better selectivity [24]. The Q-factor defines various form of quality factor that relates energy loss in reactive component to the energy stored during a signal cycle [25]. The loaded Q (Q_{Loaded}) refers to the Q-factor of a circuit while connected to external circuits as shown in equation (2.1) and (2.2).

$$Q_{Loaded} = \frac{Energy\ stored\ in\ component}{Total\ energy\ dissipate\ in\ component\ \&\ external\ circuit} \quad (2.1)$$

$$Q_{Loaded} = \frac{f_o}{3dB\ BW} \quad (2.2)$$

Q-factor is also a ratio of component's series reactance to its series resistance as shown in equation (2.3).

$$Q = \frac{X_s}{R_s} \quad \text{, when } Z_s = R_s + jX_s \quad (2.3)$$

A filter can also defined by its sensitivity, which is a measure of detector's capability to detect very small signal in presence of system noise and its acceptable signal detection is parameterized by SNR.

2.1.2 Power Amplifier

Power amplifiers convert low-power RF signals into signal with higher power. In wireless transceivers, power amplifiers take a large portion of energy consumption. Improvement of the power efficiency for PA is important for mobile application with limited battery life. Several parameters that are optimized in PA design include gain compression, linearity (OIP3), return loss on the input and output, gain, and heat dissipation.

2.1.3 Mixer (Up/Down Converter)

Mixers are electronic devices that multiply two input signals and convert them to a different frequency. There are three ports on a mixer: 1) radio frequency (RF) port where the high frequency signal is applied or produced, 2) intermediate frequency (IF) port where the low frequency signal is applied or produced and 3) local oscillator port where the RF power is applied. This process is also known as

heterodyning which is useful for modulation and demodulation. At the transmitter, the baseband signal is up-converted to a higher frequency and at the receiver the signal is down-converted to a lower frequency.

2.1.4 Impedance Matching

Matching networks maximize RF power transfer between one system or component and another. The purpose of impedance matching is to match two different terminations through a specified passband characteristic. Ideal impedance matching requires that the source and load impedances are compex conjugates [26].

Matching networks can have low-pass characteristics (series inductor and/or shunt capacitor), high-pass characteristics (series capacitor and/or shunt inductor). It could also have band-pass or band-stop characteristics which is a combination of low-pass and high-pass characteristics.

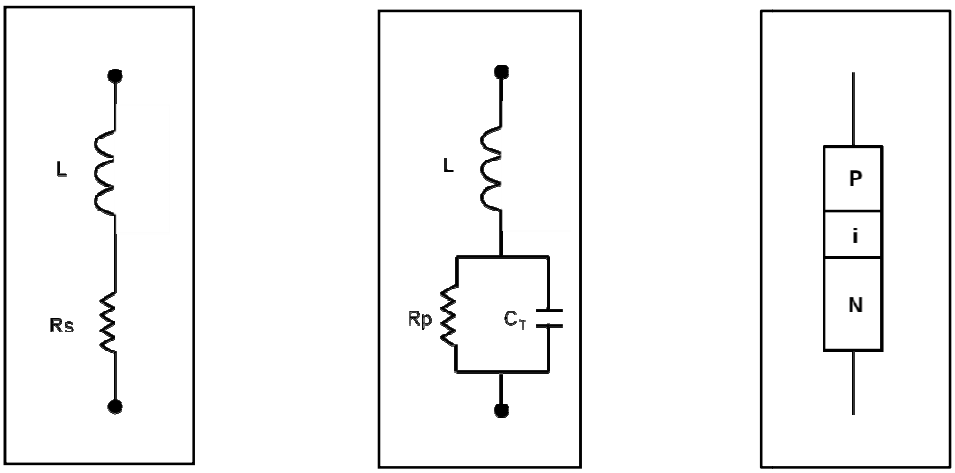
2.2 Microwave Switches

This section discusses several microwave switches in terms of how they function, the equivalent circuit models, the advantages and disadvantages.

2.2.1 PIN Diode

PIN diode is a semiconductor device that operates as a variable resistor at RF and microwave frequencies. Its resistance value is determined by forward biased dc current [27 – 28]. Its important feature is the ability to control large RF signal with a small dc bias.

PIN diode consists of 3 semiconductor regions: p-type, n-type and semiconductor region with lightly doped intrinsic semiconductor region (insulator) in between them used to linearize the diode. The intrinsic region increases the breakdown voltage that enables PIN diode to deal with high input power. The equivalent circuit of PIN diode is shown in Figure 2.3.



(a) Forward Bias (ON) (b) Reverse Bias (OFF) (c) Cross Section

Figure 2.3 Equivalent Circuit of PIN Diode

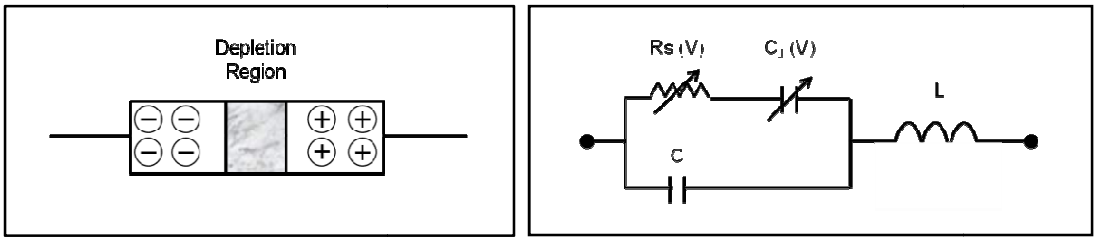
In switching application, low-impedance is obtained by operating it under forward bias (ON state). While a low-capacitance as an RF choke is obtained by operating it under zero/reverse bias (OFF state) [28].

As a switching device, PIN diode switching speed is relatively slow on the order of microseconds due to the capacitive region (insulator) between the p-doped and n-doped regions. In the circuit, PIN diodes rectify the RF signal and the isolation is not very high [29]. PIN diode is available as through-hole component.

2.2.2 Varactor Diode

Varactors are semiconductor diodes with the properties of voltage-controlled capacitor and series resistor. The width of depletion region, which acts as junction capacitance varies as a function of applied voltage. The capacitance of varactor diode varies with the reverse voltage [25], [30] – [31].

When reverse bias is applied at varactor, the thickness of depletion zone will vary with the input voltage and so will the capacitance. The reverse-voltage applied on the varactor is usually within the range of 10 – 20 V. Varactor diode allows faster tuning speed in the order of nanoseconds. However, varactor diode introduces more insertion loss and less isolation. It also highly non-linear and has lower power handling capability.



(a) Depletion Layer (b) Equivalent Circuit

Figure 2.4 Equivalent Circuit of Varactor Diode

2.2.3 MEMS Switch

MEMS stand for Micro Electro-Mechanical System. MEMS devices use mechanical movement to achieve short circuit or open circuit in transmission line. MEMS switches obtain its force by electrostatic, magnetostatic, piezoelectric or thermal design. Some applications of RF MEMS are phase shifters, antenna application, tunable filter and switches [32] – [33].

MEMS techniques allow both electronic circuits and mechanical devices to be manufactured on a silicon chip. The followings are 3 main processes in MEMS development [20]:

1. Deposition processes result in the deposit of thin films on the substrate. Deposition occurs due to various chemical or physical reactions.
2. Lithography is a patterning process on a photosensitive material by selective exposure to a radiation source.
3. Etching processes are used on the films deposited to form the functional MEMS structure. Etching either occurs by wet etching or dry etching.

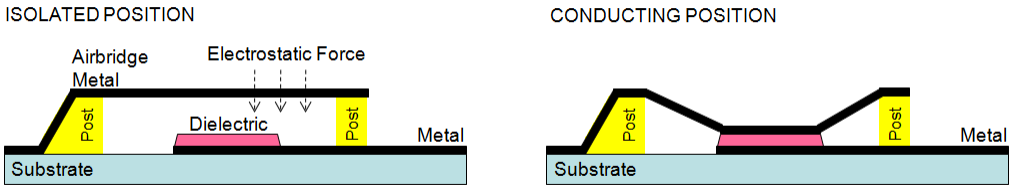


Figure 2.5 Cross Section of MEMS [3]

Micro-electro-mechanical systems (MEMS) suit to build variable capacitors and RF switch [3]. MEMS have been used widely for many tunable filter designs. RF MEMS switches offer superior performance compared to other microwave switches in terms of isolation, insertion loss, linearity and power consumption. However, the limitation of RF MEMS switches come from its low switching speed (2 – 40 μs), reliability, high voltage drive (20 – 100 V) and high production cost [34] – [35]. One unit of MEMS SPDT costs USD 25 – 92. MEMS implemented on CMOS have large parasitic, size limitation and high loss [29], [36] – [38].

2.2.4 GaAs MESFET

Field Effect Transistor (FET) are most commonly used to fabricate a switch in monolithic microwave integrated circuit (MMIC) applications [38]. As a microwave switch, the RF passes between transmitted from the source to drain contact and the gate acts as the control terminal [30], [39] – [41]. FET switch only requires voltage signal for switching, therefore no additional DC power consumed for switching [42].

There are numerous FET with different sizes and number of fingers. Geometry of the switch is designed such that the parasitic effects (series inductance, phase dispersion and capacitance to ground) are minimized to reduce distortion effect to the input signal. The work on development of MMIC switch models has been reported in [43]. The theory indicates that FET switch should be able to provide good performance at milimetre-frequency, but the problem is the implementation of the device and circuit such that it achieves low loss, high isolation and good power handling capability at high operating frequencies [44] – [45].

The typical gate bias resistor value is 2 – 8 kΩ. The switch performance is limited by the small capacitance at the off-state (C_{DS}) that causes loss of isolation. At very high frequency, the existence of C_{DS} degrades the performance of the switch as an open circuit (OFF state). Figure 2.6 shows the equivalent circuit for FET switch.

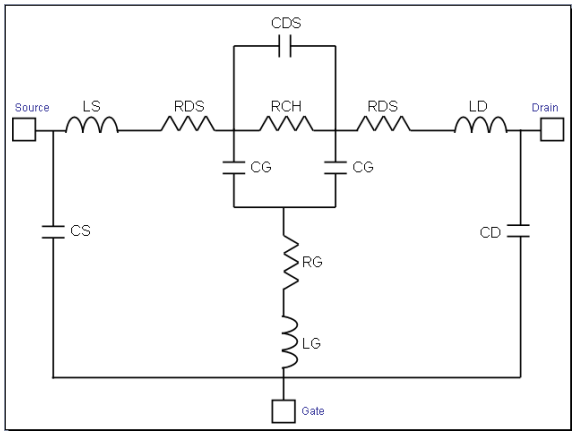
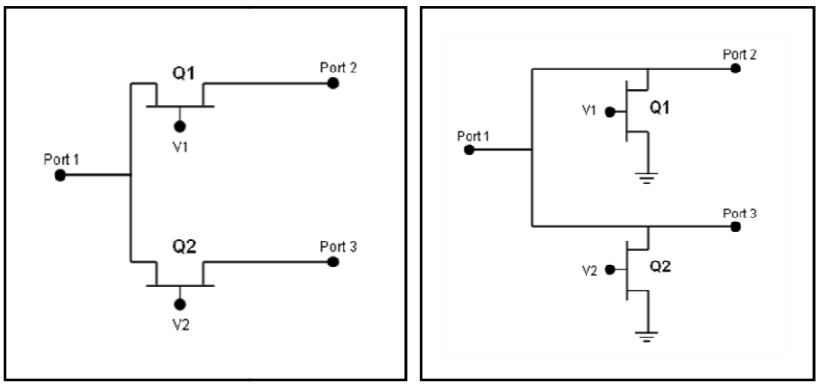


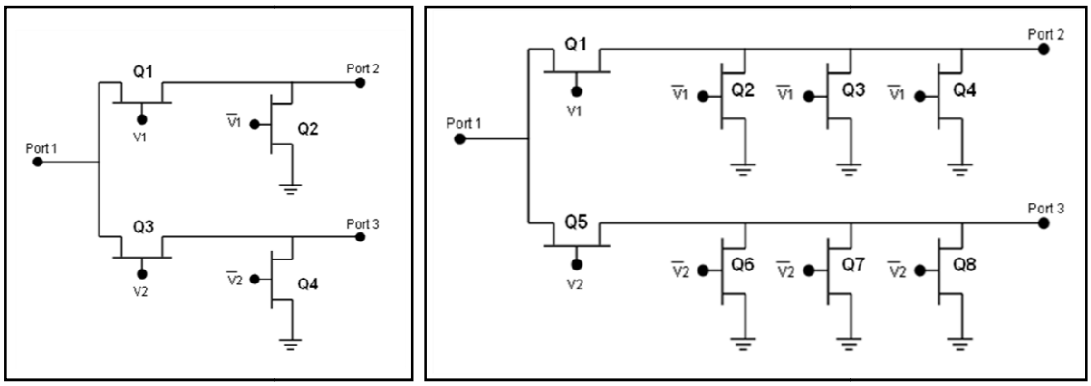
Figure 2.6 Equivalent Circuit for FET Switch

When the transistor is in its OFF state, the channel resistance (R_{CH}) value is very large hence drain to source is open circuited. When the transistor is in its ON state, the value of (R_{CH}) is considerably small hence the drain to source is short circuited with a little conductor loss. The drain-to-source capacitance (C_{DS}) does not vary much between the ON and OFF state. However, the gate capacitance (C_G) gives some contribution for the resonant frequency tuning as it varies between 0.5 pF (ON state) to 0.085pF (OFF state) for 4-fingers FET.

The followings show several common switch design topologies to realize SPST or SPDT switches using GaAs FET [45] – [52].



(a) 1-Stage Series SPDT (b) 1-Stage Shunt SPDT



(c) 1-Stage Series-Shunt SPDT (d) Distributed SPDT

Figure 2.7 Common topologies used in switch design

A study case on single, double and triple-gate FET switches were performed using the WIN PD 50-01 device model. Multiple-gate switches are larger structures with wider separation between the source and drain terminals that cause the signal to travel longer distance and results in higher R_{CH}. Due to this large separation, the value of drain to source capacitance (C_{DS}) is lower for multiple gate switches. Therefore, multiple-gate switches connected using a series topology introduce higher on-state insertion loss but improve off-state isolation. Figure 2.8 shows the on-state insertion loss (0.40 dB, 0.55 dB, 0.70 dB) and off-state isolation (10 dB, 17 dB, 20 dB) for single-gate, dual-gate and triple-gate FET switch, respectively.

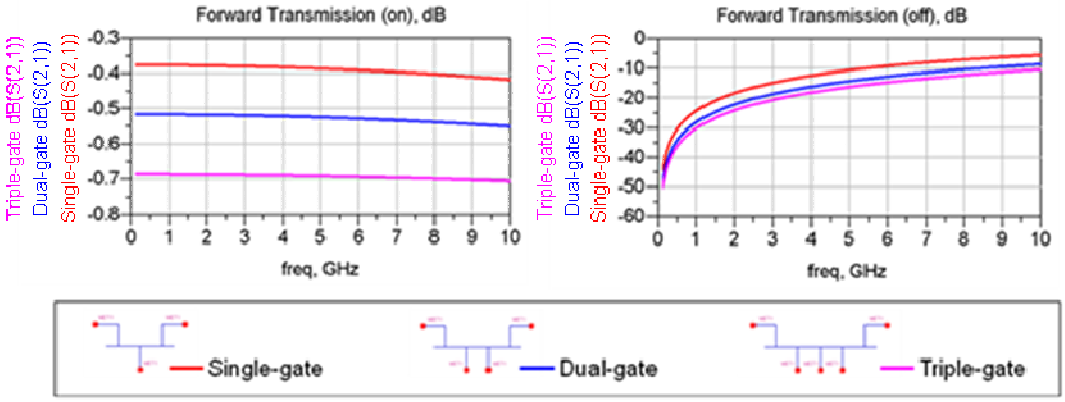


Figure 2.8 Performance Comparison of Multiple-gate Switches

2.2.5 Comparison of Microwave Switches

Table 2.1 shows the comparison of several microwave switches that were used in works related to realization of reconfigurable devices.

Table 2.1 Comparison of Some Microwave Switches [53] – [56]

	MEMS [53] (James Brank, May 2001)	**Varactor** [54] (B. Kapilevich, April 2007)	**PIN Diode** [55] (C. Lugo Jr., December 2004)	**RF Relay** [56] (William Sabin, Oct 2000)
Center Freq. (f_o)	110 – 160 MHz	1.1 – 1.5 GHz	5.8 GHz	0.1592 Hz
Bandwidth	37 – 58MHz (± 28.6%)	24 – 37MHz (± 2.3%)	315 – 587 MHz (± 7.77%)	± 0.0159 Hz (± 9.98%)
Insertion Loss	3.7 – 4.2 dB	3 – 4.5 dB	± 0.51 dB	< 2 dB
Return Loss	> 10dB	± 15dB	± 10dB	very small
DC bias	± 100 V	1 – 12 V	Forward bias 20 mA Reverse bias -10 V	low
Size	(± 1 – 100 μm)	± 5 – 15cm	± 1 – 2 mm	5 x 7 x 2 inch
Remark	• Expensive • Relatively new • Require very high dc biasing • Cannot be implemented monolithically	• Implementation using microstrip/ stepped impedance • Require large dc biasing circuitry • Relatively non-linear	• Implementation using microstrip • Cannot be implemented monolithically	• Very large • Cannot be implemented monolithically • High power handling up to 10W & OIP3 up to 57 dBm • Slow switching speed

2.3 Development of Adaptive System

Tunable front end allows a single module to be capable of being intelligent in utilizing several designated transmit and receive frequency bands. It is important that

the components for this front end be electronically tunable. Also, every stage of the RF design must be matched properly to previous and subsequent stages and has to meet the required specifications [2].

2.3.1 Adaptive Microwave Filter

Electronically tunable or reconfigurable microwave filters is one of the most popular research in the development of adaptive microwave system [26], [57] – [62]. Based on reference [63], the development of adaptive filter is categorized into several classes, listed as:

1. Filter with variable bandwidth
2. Filter with variable center frequency
3. Filter with variable skirt selectivity
4. Filter with variable group delay-equalization

Traditionally, to vary the center frequency, adaptive function of filters is achieved by stacking a set of fixed-frequency filters and performs cold switching. The duplication of functions using this approach causes the circuit size to be large, inefficient, and costly, which is not suitable for portable devices.

Combline filter structure is widely used together with the tuning elements such as semiconductor PIN and varactor diodes, RF MEMS and other material-based components [26]. Many works replace the capacitive elements with tunable capacitors like varactor, a voltage-controlled capacitor, to allow frequency tuning. However, varactors introduce nonlinearities at high power levels. Varactors also limit the loaded quality factor Q as a function of intrinsic impedance, transmission line impedance and the varactor series resistance [26], [57].

MEMS switches offer higher performance up to 120 GHz (i.e. high isolation, low insertion loss, high Q factor and high linearity) compared to PIN diode or FET switches. These advantages encourage more research and work on tunable and reconfigurable system using MEMS switch. However, the development of MEMS packaging has not matured yet. Many research works are ongoing to improve MEMS yield and repeatability and to investigate the environmental robustness [64].

Recently, active filtering techniques have been proposed where the filter structures employ combinations of both passive and active elements. This loss compensation technique intends to serve its purpose as a filter and neutralize the effect of circuit losses at the same time. An approach to compensate loss is the use of negative resistance to compensate passive element and tuning element losses. Under small signal condition, this approach could achieve lossless filter response with large tuning range. However, nonlinear-related problems such as intermodulation distortion and device saturation occur for high power operation [57].

2.3.2 Adaptive Microwave Power Amplifier

Another area currently under development is tunable and reconfigurable power amplifiers. Reference [4] defines several categories of adaptive amplifier as follow:

1. Adaptive PA with variable microwave output frequency.
   In commercial applications, a number of standards occupy spectral bands such as GSM, GPRS, EDGE, CDMA, UMTS, WiMAX, etc. In military applications, the research work towards realizing single radio that is capable to operate in wide variety of frequencies and waveforms.
2. Adaptive PA with variable output power level.
   It is desired to have control over the output power of a transmitter to correspond to the varying needs of the link to conserve power and to avoid excessive interference to other users of the spectrum.
3. Adaptive PA with variable modulation formats.
   The amplifier changes to satisfy the required trade-off of linearity and efficiency as output signal is changed between different modulation formats.
4. Adaptive PA with variable antenna impedances.
   The amplifier changes its output impedances as the variation of antenna impedances.
5. Adaptive PA with variable interference sources and constraints.
   In the crowded frequency band, it is desired that the amplifiers in the receivers be able to filter out interferences and harmonics that are detected in

various frequencies. The amplifiers in the transmitters are also required to filter their out-of-band components to avoid co-site interference and self-jamming. If there is an interfering signal near the operating band, in-band distortion can occur in the receive channel via the cross-modulation process.

In its development, tunability is used not only to shift the operating frequency but also to realize broadband power amplifier and to improve Power Added Efficiency (PAE) and linearity [9], [12], [13], [16], [65], [66]. Many works integrate tuning elements in the output matching network to obtain optimum resistance at antenna impedance. Some works also integrate tuning elements at the input matching network to boost the power gain. Use of passive elements in tunable matching network as an integral part of power amplifier does not consume additional DC power.

Other works reported by [10] – [11] propose multi-band PA module for reconfigurable RF Front-End architecture. The control components used in these works are coupled inductors, PIN diodes, varactors and MEMS.

The realization of tuning elements integrated into the power amplifiers was achieved using surface-mount components [6] or monolithically [19]. However, in [19], the power amplifier, the input matching network and output matching network were fabricated in 3 different die and they were connected using bondwires. Another approach for reconfigurable system blocks might be realized monolithically in a single die with integrated tuning elements. Monolithic integration of system block and the control components result in smaller size of the overall circuit and lower production cost.

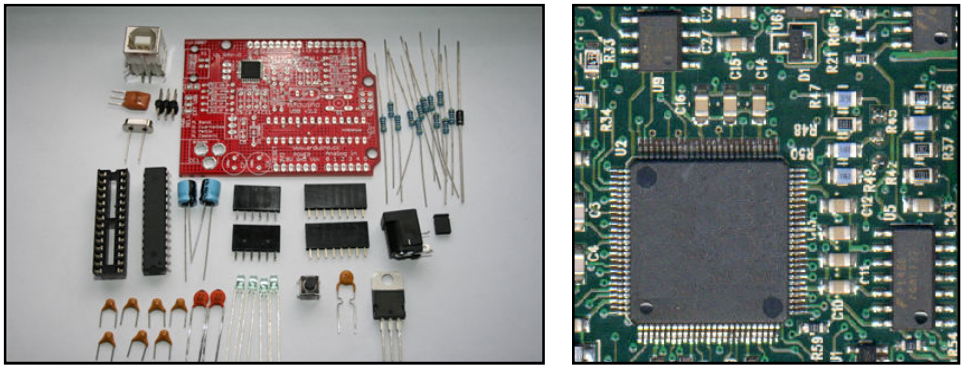
2.4 The Technology

The following sections discuss two type of technologies employed in the fabrication process for this work: 1) Surface-Mount Technology (SMT) and 2) Monolithic Microwave Integrated Circuits (MMIC).

2.4.1 Surface-Mount Technology (SMT)

Surface-mount technology is a type of electronic component package in which the components are designed to be mounted and soldered on the conductive surface of a PCB. Mounting scheme of through-hole components involves pins inserted to plated-through-hole drilled in printed circuit board (PCB) and soldered to the pads on the other side of the PCB. Figure 2.9 (a) and (b) show the through-hole and surface-mount components. The following are several benefits of SMT over through-hole technology:

1. Smaller physical size for same electrical function.
2. At RF signals, parasitic effects are smaller so component characteristics are easier to predict.
3. Cheaper raw material cost.
4. Better mechanical performance under shake and vibration condition due to lower mass.
5. Faster and simpler for automated assembly.



(a) Through-hole Components (b) Surface-mount Components

Figure 2.9 Through-hole and Surface-mount Technology

Along with the development of SMT, other technology enhancements are also growing, such as solder paste maturity, substrate material enhancement, alternate lead form, standardized package types, etc.

Normally, vendors of surface-mount devices (SMD) provide the equivalent circuit model or measured S-parameters to support the clients in design process.

2.4.2 Monolithic Microwave Integrated Circuits (MMIC)

Monolithic Microwave Integrated Circuits (MMIC) are circuits that operates at microwave frequencies (300 MHz to 300 GHz). MMICs are dimensionally small (about 1 – 10 mm^2) and are easily be mass produced.

The oldest Gallium Arsenide (GaAs) technology, MESFETs, is commonly used to implement switches and some power amplifiers. This well-established process offers reliability and good noise performance. On other hand, GaAs HBT (Heterojunction Bipolar Transistor) technology offers better performance for power amplifier and high linearity. This technology is often fabricated using InGaP.

Compared to the earlier technologies, pHEMT devices generally offer lower noise performance and have been used for high sensitivity applications such as GPS receivers. Gallium Nitride (GaN) supports higher power application [23].

The active and passive components of MMIC can be fabricated on the same semiconductor substrate. However, special devices such as Gunn diodes, PIN diodes switches and varactor diodes are rarely incorporated into MMIC processes [20], [42].

Reproducibility and circuit yield are excellent for MMICs because the active and passive components are produced by the same well-controlled fabrication steps, using the same photolithographic masks. MMICs are very compact in terms of size and mass. In comparison, the hybrid MIC suffers from device placement and wire bonding variations from circuit to circuit which results in higher parasitic effects. These make the MMICs more reliable than hybrid circuits. The mechanical limitations of chip attachment and wire-bonding become too apparent when a hybrid circuit is subjected to temperature cycling, shock and vibration.

2.5 Performance Parameters

This section discusses the parameters that are used to analyze the circuit performance. The variables used to describe the performance parameters are defined below.

P_{out} Output Power

P_{in} Input Power

P_{inc} Power available from source

P_{load} Power delivered to load

P_{LR} Power Loss Ratio

P_{DC} DC Power

Z_0 Characteristics impedance

Z_L Load impedance

RL Return Loss

2.5.1 Gain

Amplifier gain is the ratio of output to input power which is usually measured in decibels (dB) [25].

$$G(dB) = 10\log\left|\frac{P_{out}}{P_{in}}\right| \tag{2.4}$$

2.5.2 Insertion Loss

One way to design a filter is by using insertion loss method in which a filter response is defined by its insertion loss (IL) or power loss ratio (P_{LR}) [25].

$$P_{LR} = \frac{Power\ available\ from\ source}{Power\ delivered\ to\ load} = \frac{P_{inc}}{P_{load}} = \frac{1}{1-\left|\Gamma(\omega)\right|^2} \tag{2.5}$$

The insertion loss in dB is

$$IL(dB) = -10\log\left|P_{LR}\right| \tag{2.6}$$

2.5.3 Return Loss

The amplitude of the reflected voltage wave normalized to the amplitude of the incident voltage wave is defined as the voltage reflection coefficient, Γ:

$$\Gamma = \frac{V_o^-}{V_o^+} = \frac{Z_L - Z_o}{Z_L + Z_o} \qquad \text{, where } Z_L = R_L + jX_L \tag{2.7}$$

When the load is mismatched, not all of the available power from the generator is delivered to the load. This loss is called return loss (*RL*). If Γ = 0, maximum power is delivered to the load and its return loss in dB. While Γ = 1 means total reflection or no power is delivered to the load [25].

$$RL(dB) = -20\log|\Gamma| \tag{2.8}$$

2.5.4 Rejection

Reconfigurable power amplifier can operate in several center frequencies or states. The gain difference (dB) between a particular center frequency and the maximum gain is the rejection.

2.5.5 Bandwidth (BW)

Bandwidth (BW) represents the range of frequencies that the PA is most effective in amplifying. The common and well accepted metric to define the operating bandwidth is the *half power points* that indicate the points with half of the peak output power (3 dB differences). Referring to Figure 2.10, difference between f_1 and f_2 defines the 3dB-bandwidth of the amplifier [67].

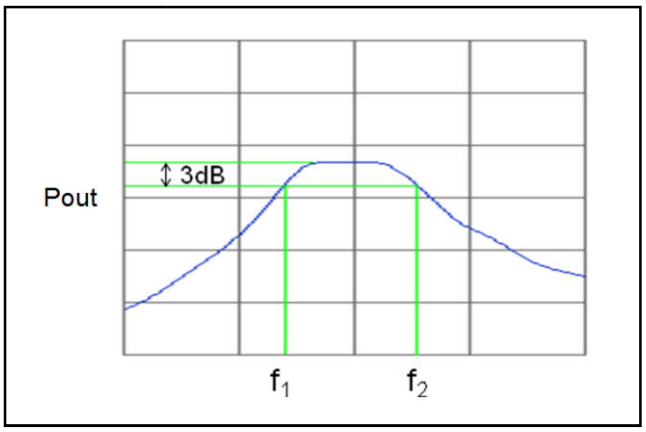


Figure 2.10 Half Power Point to Determine Bandwidth

2.5.6 Gain Compression (P_{1dB})

P_{1dB} is one parameter to measure output power. The P_{1dB} value can be determined by plotting the measured response and ideal linear response of output power [67] – [68]. P_{1dB} is the input power where these two lines diverge by 1 dB (the gain drops by 1dB).

Figure 2.11 shows the plot of input/output characteristics of a device whose gain is 13 dB for input power up to -6 dBm. As the input power increases, the output power begins to saturate and the gain begins to drop. At P_{in} = -2 dBm, the gain drop is exactly 1 dB and the P_{1dB} of the device at the output power is 10 dBm.

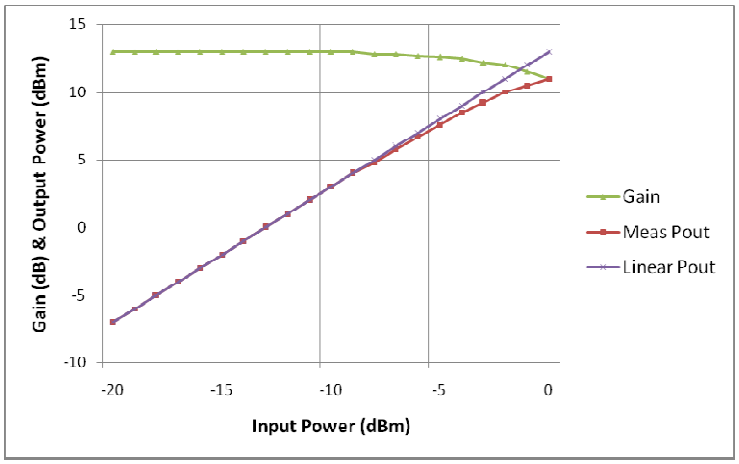


Figure 2.11 Gain and Output Power vs. Input Power

2.5.7 Linearity (OIP3)

When two tones of input are input to non-linear device, intermodulation products are generated [69]. These products are the sum and difference of multiples of the fundamental tones. The harmonics that are out-of-band cause no problems. However, the third-order differences tones are nearest to the fundamentals as shown in Figure 2.12. Third-order intercept point relates non-linear products caused by the third-order nonlinear term to the linearly amplified signal [70]. Third order intercept point is 10 to 20 dB higher than P_{1dB} gain compression point [71].

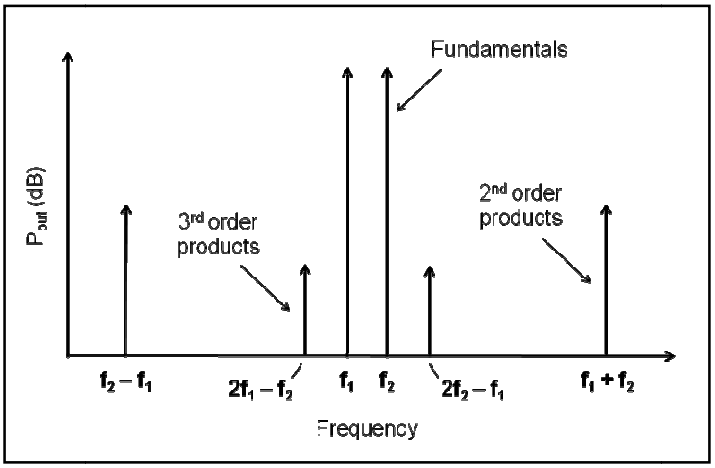


Figure 2.12 Fundamentals and Intermodulation Products

2.5.8 Stability

In microwave amplifier design, stability issue must be taken into design process to avoid oscillation. Oscillations are possible if either the input or output port impedance has a negative real part which implies that $|\Gamma_{in}| > 1$ or $|\Gamma_{out}| > 1$. The followings are two most common stability conditions [25]:

1. Unconditional stability

   The network is unconditionally stable if $|\Gamma_{in}| < 1$ and $|\Gamma_{out}| < 1$ for all passive source and load impedance.

2. Conditional stability (Potentially unstable)

   The network is conditionally stable if $|\Gamma_{in}| < 1$ and $|\Gamma_{out}| < 1$ for only a certain range of passive source and load impedances.

Several tests could be employed to determine unconditional stability such as stability circles test and $K - \Delta$ test (Rollet's Condition). Recent study by [72] reported that a stability test can be performed on a multifunctional circuit. The two steps to observe the stability are: 1) stability analysis at nominal operation point for both small and large signal, 2) study of steady-state oscillatory solution.

2.5.9 Power Added Efficiency (PAE)

Power amplifier usually consumes the most DC power in portable wireless devices, so amplifier efficiency is a very important consideration. One measure of amplifier efficiency is defined by power added efficiency (PAE) [25].

$$\eta_{PAE} = PAE = \frac{P_{out} - P_{in}}{Total\, P_{DC}} \tag{2.9}$$

2.5.10 Mismatch Loss

Mismatch loss is the amount of power dissipated between two interconnected ports. In a lossless matching circuit, mismatch factor is an invariant quantity. For two interconnected ports where $Z_1 = R_1 + jX_1$ is the impedance at the input and $Z_2 = R_2 + jX_2$ is the impedance looking towards output, the mismatch factor is shown in equation (2.10) [73].

$$M = \frac{4R_1R_2}{\left|Z_1 + Z_2\right|^2} \tag{2.10}$$

This chapter starts with the discussion of the existing RF front end system and architecture in the transmitter and receiver side. Several common microwave switches used in the recent research works to achieve reconfigurability in RF front end are described. The next section describes the development of adaptive system for some primary components in RF front end. The developing trend of adaptive

microwave filter and adaptive power amplifier are elaborated. The following section explains the technologies used in this project (Surface-mount technology and MMIC technology) to realize the reconfigurable power amplifier. Finally, several performance parameters including the formulas are described in this chapter.

CHAPTER 3

METHODOLOGY

This chapter describes the steps taken to achieve the objectives which include the design process, experimental setup and measurements. It covers the techniques and methods utilized throughout this project.

A block diagram of the tunable matching network shown in Figure 3.1 is integrated into the interstage of a 2-stage power amplifier to provide the capability of center frequency tuning. The two main designs described in this chapter are a discrete design and a quasi-MMIC design.

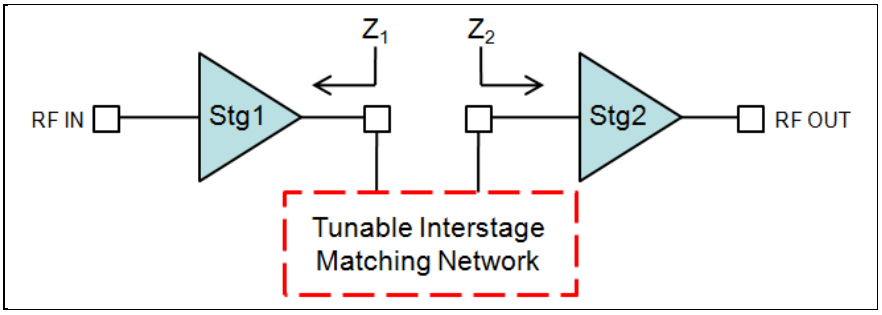
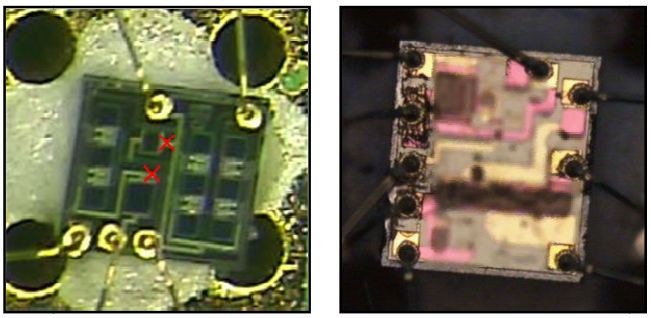


Figure 3.1 Tunable Interstage Matching Network

These matching networks were designed for two 2-stage power amplifiers, Amp_A and Amp_B. Amp_A is an existing amplifier that was not designed specifically for this project. The interstage of Amp_A was removed using a laser to isolate the first and second stages so that no interference is introduced to the new tunable interstage. The crosses shown in Figure 3.2 (a) indicate the lines removed using a laser. Amp_B, shown in Figure 3.2 (b), was specifically designed without an interstage matching network and an opening between the stage 1 and stage 2 amplifiers was provided using bond pads for external matching network.



(a) Amp_A (b) Amp_B

Figure 3.2 Two-stage Amplifiers

3.1 Circuit Design Methodology

The first step is the circuit design including device selection for stage-1 and stage-2 amplifier, ballast and biasing network, and input / output matching network is discussed in Section 3.1.1. Two different methods, using the Smith chart and exploitation of the interstage mismatch, are employed in designing the interstage matching network for tuning. The graphical method using Smith chart determines the structure or topology of interstage matching network including its initial (lossless) component values. The mismatch analysis is used to re-tune the component values in the interstage that achieves equalized gain responses at different tuning states. The methods are complementary to each other and they will be described in Section 3.1.2 and 3.1.3.

3.1.1 Initial Circuit Design

In the initial circuit design, the first step is to select the active devices (HBT/FET) for first and second stage amplifier. Amp_A was designed using the H02U-41 InGaP/GaAs HBT model provided by WIN Semiconductor. The device used is 320 μm^2 for stage-1 and 640 μm^2 for stage-2 (each transistor is 2 $\mu m \times 20$ $\mu m \times 2$ fingers).

Each cell in the amplifier uses a high-pass network structure (series resistor with parallel by-pass capacitor) placed at the input of the transistor as shown in Figure 3.3. These high-pass networks located at the base of the transistors effectively

reduce the gain. The reduction in high-frequency gain however, can be minimized with a parallel capacitor resulting in a relatively more flat wideband response across the operating frequency band [76]. At low frequency, the signal sees the capacitor as an open circuit and mostly flows through the resistor. The resistive loading reduces the low frequency gain and at the same time improves its stability. At high frequency, the signal mostly flows through the bypass capacitor instead of the resistor resulting in only a small amount of gain reduction at higher frequencies. This capacitor is added in parallel with the stabilizing resistor in each cell to trade-off the low frequency gain with the high frequency gain.

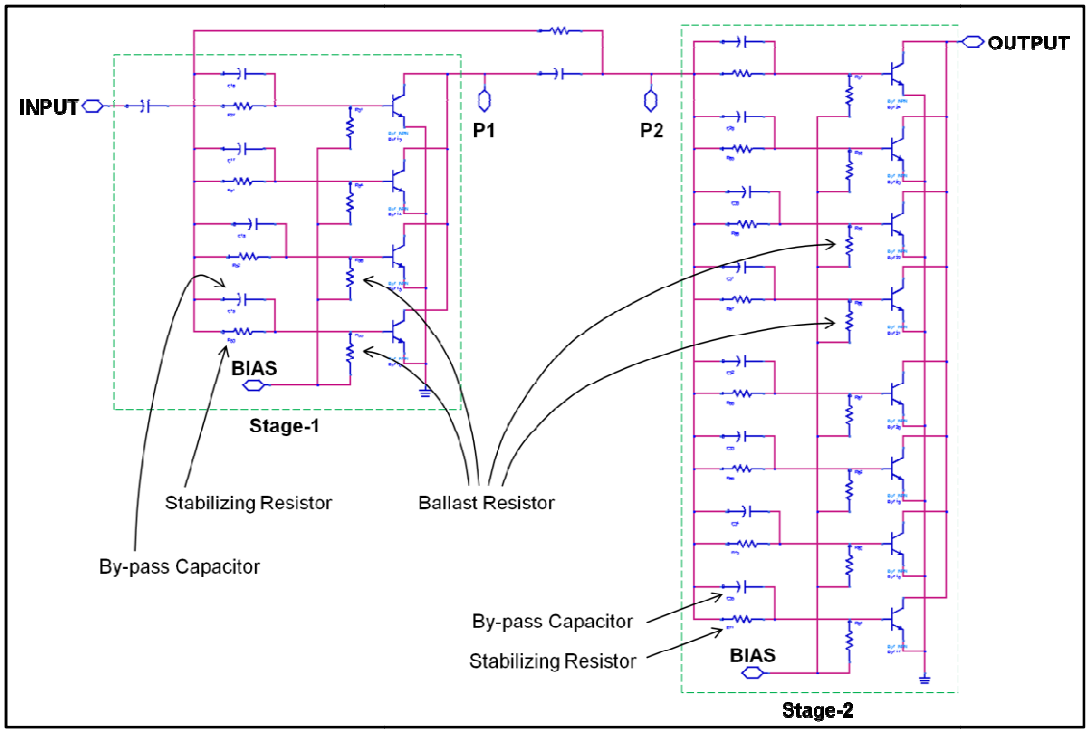


Figure 3.3 Schematic Diagram of Two-Stage Amp_A

For high output power, several HBTs must be connected in parallel. When thermal runaway occurs for many HBT devices connected in parallel, a single HBT with the highest temperature eventually draws more current and all of the current ends up flowing through only a single HBT. A method to avoid this phenomenon is to use a separate ballast resistor for each HBT since each HBT has a different DC operating point.

In the initial design, the stage-1 is connected to the stage-2 amplifier using a blocking capacitor to prevent dc current through the interstage and a feedback resistor is placed to improve stability.

Thermal runaway is a condition where an increase in the device temperature causes a further increment in the current flowing through the transistor (I_C), which eventually can cause device failure. To avoid thermal runaway, ballasting network is included in each HBT cell in both stage-1 and stage-2 amplifiers. Base ballasting uses a resistor in series with the base dc biasing to control the transistor state. When the device temperature increases, the transistor draws higher base current ($I_B = I_C$ / ß) that increases voltage across ballast resistor (V_{bb}). By KVL around the loop (Figure 3.4), the V_{BE} decreases thus preventing the thermal runaway. The device will be turned off if it draws high enough current that cause the base-emitter voltage (V_{BE}) to be less than the threshold voltage ($E_B - V_{bb} < V_{Th}$).

$$E_B = V_{bb} - V_{BE} \tag{3.1}$$

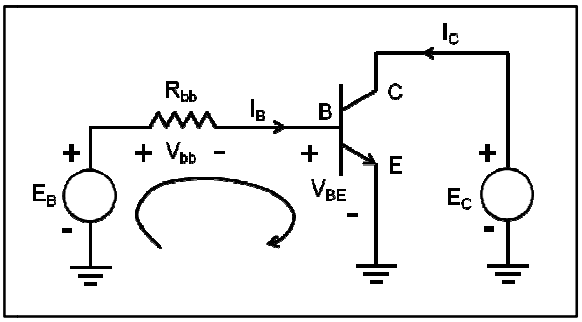


Figure 3.4 Base Ballasting for HBT

The layout of Amp_A MMIC is shown in Figure 3.5. The two stage amplifier with blocking capacitor at the interstage and the parallel ballasting were laid out on a die with the dimension of 720 µm × 660 µm. Originally, this amplifier was designed as a standard two-stage amplifier. The capacitor and resistor in the interstage were removed using laser as indicated by the crosses in Figure 3.5 to cater for the design of reconfigurable power amplifier with tunable interstage matching network.

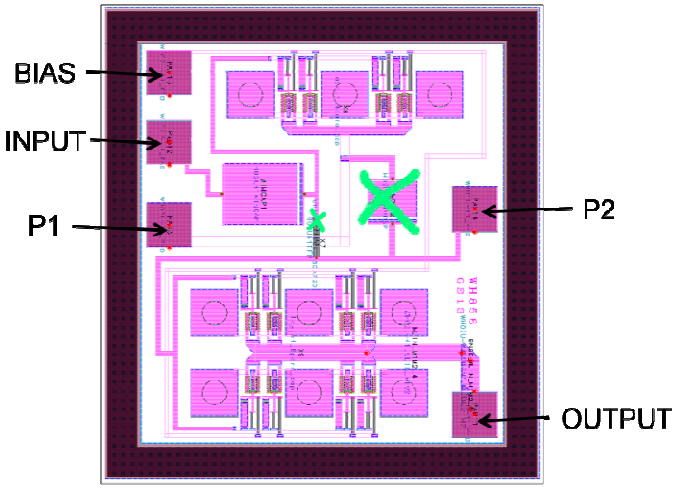


Figure 3.5 MMIC Layout of Amp_A

The input matching network of Amp_A is a simple high-pass L-section (series capacitor and shunt inductor) and the output matching network used is a low-pass L-section (series inductor and shunt capacitor).

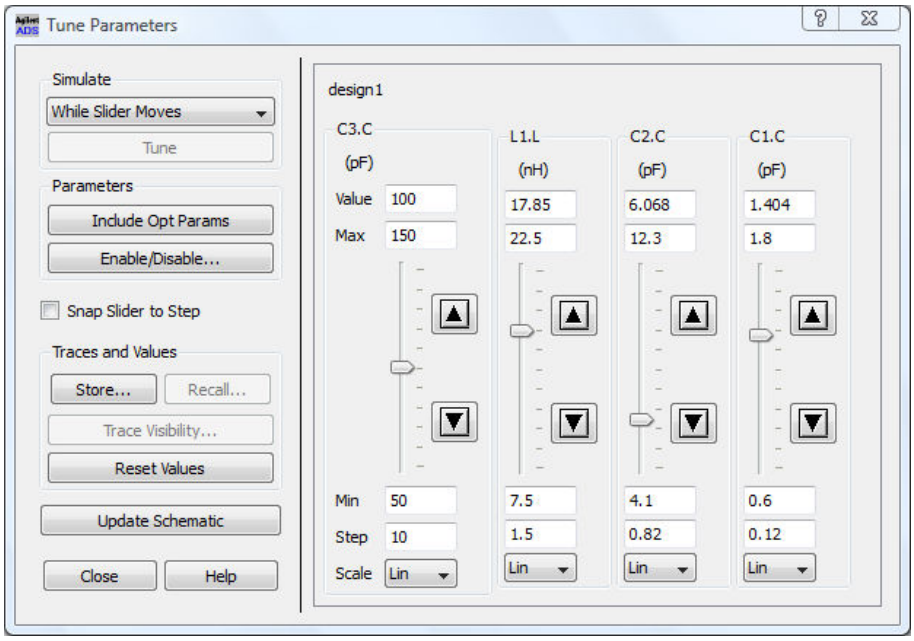


Figure 3.6 Tune Parameters in ADS

The initial input and output matching networks were designed using ideal components in Agilent's Advanced Design System (ADS). Two approaches were used to optimize the component values: 1) ADS Performance Optimizer, and 2)

Tune Parameters. In this work, only the Tune Parameters approach was used to optimize these component values (Figure 3.6).

The component values used in the input, output and interstage matching networks were tuned manually while observing the S-parameter performance. After the initial component values were optimized, the ideal components were then replaced with the actual component models. The discrete component models were provided by Johanson, Skyworks, and Coilcraft and the MMIC component models were provided by WIN Semiconductor.

The initial value of input and output matching network provides a wideband matching for the operating frequency band and the response for Amp_A has a relatively flat gain (S_{21}) of 10 dB from 0.5 GHz to 2.5 GHz.

3.1.2 Graphical Method using Smith Chart

The next step is used to determine the structure (topology) of interstage matching network that has a bandpass response. The graphical method using Smith Chart obtains the initial component values for the interstage matching network.

The following example is taken from variant DTN2 that uses T-section topology for the interstage and is realized using discrete components. First, one has to examine the impedances looking towards the output of first stage amplifier (Z_1) and towards the input of second stage amplifier (Z_2). The impedances are tabulated in Table 3.1.

Table 3.1 Impedances Z_1 and Z_2 for DTN2 Design

Frequency (f_o)	Z_1	Z_2
200 MHz	178.15 – j245.80	22.50 – j4.50
300 MHz	116.05 – j214.25	22.80 – j4.85
400 MHz	82.30 – j186.70	22.80 – j5.35
500 MHz	57.15 – j158.65	23.95 – j5.95
700 MHz	28.90 – j113.10	25.95 – j7.00

Ideally, to ensure optimum power transfer, Z_2 at the operating frequency is transformed to the Z_1*. However, impedance Z_2 is transformed to Z_T whose

difference from Z_1* can be exploited to equalize gain. Transformation to the high reactance (high-Q) region of the Smith chart is necessary to provide minimum bandwidth.

The T-section interstage matching network consists of series capacitor, shunt capacitor and large series inductor. A 4-way switch is used to switch between four inductor values to vary the interstage impedance. The following calculation shows the impedance transformation using T-section interstage matching network in variant DTN2 at frequency 200 MHz (refer to Figure 3.7).

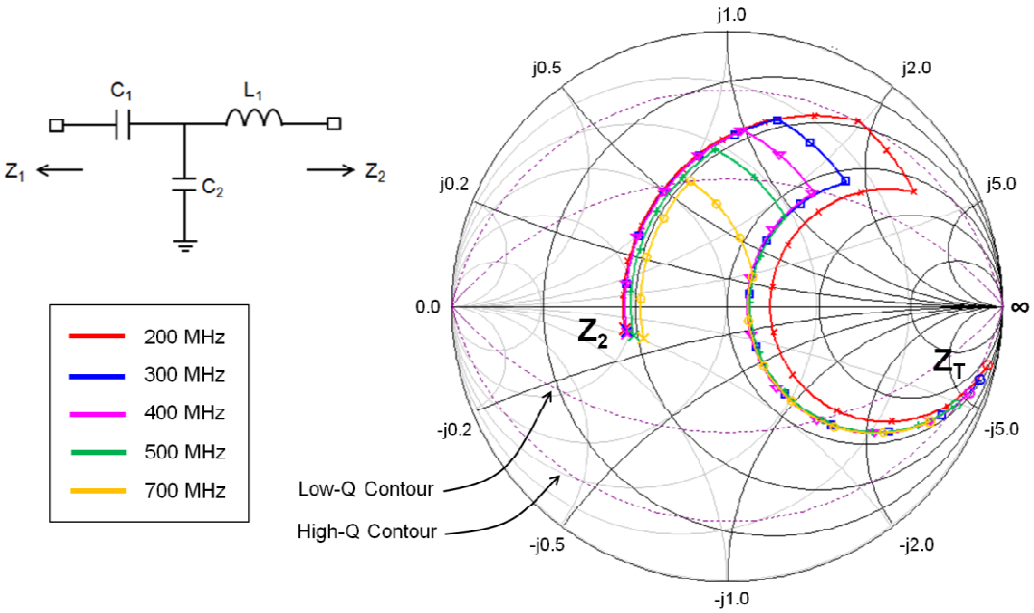


Figure 3.7 Interstage impedances transformation for DTN2 with Amp_B (T-section)

$f_0 = 200\ MHz$

$Z_2 = 22.50 - j4.50\ \Omega$

Series Inductor $L_1 = 68\ nH$ takes Z_2 to Z_A:

$X_{L1} = j\omega L_1 = j(2\pi 200MHz)(68nH) = j85.45\ \Omega$

$Z_A = (22.50 - j4.50) + j85.45 = 22.50 + j80.95\ \Omega$ → high-Q region

$Y_A = 1/Z_A = 0.0032 - j0.011467\ S$

Shunt Capacitor $C_2 = 8.2\ pF$ takes Z_A to Z_B:

$B_{C2} = j\omega C_2 = j(2\pi 200MHz)(8.2pF) = j0.0103\ S$

$Y_B = (0.0032 - j0.011467) + j0.0103 = 0.0032 - j0.001167\ S$

$Z_B = 1/Y_B = 275.82 + j100.60\ \Omega$

Series Capacitor $C_1 = 1.2\ pF$ takes Z_B to Z_T:

$X_{C1} = 1/j\omega C_1 = 1/j((2\pi 200MHz)(1.2pF)) = -j663.14\ \Omega$

$Z_T = (275.82 + j100.60) - j663.14 = 275.82 - j562.54\ \Omega$

In variant DTN2, a large series inductor takes point Z_2 (refer to Figure 3.7) towards the top edge of Smith chart to reach the high Q-contour. Then shunt capacitor transforms the impedance (admittance) along the constant conductance circle with clock-wise direction. The series capacitor then takes the impedance to the transformed impedances (Z_T) at each operating frequency. Figure 3.7 shows the effect of varying the series inductor in the interstage impedance matching using T-section at different frequencies. Each transformation at different operating frequency is represented by a different color.

3.1.3 Mismatch Factor for Gain Equalization

The gain roll-off analysis for these 2 amplifier stages must be performed before this interstage mismatch analysis. The gain difference between the lowest and highest operating frequencies is calculated separately for each amplifier stage. The difference in gain from both amplifiers is the amount of variation to be compensated by the interstage mismatch loss as illustrated in Figure 3.8.

Mismatch loss at the interstage matching network is observed using the M-probe technique. This probe is a noninvasive analysis probe that can be placed at arbitrary point within the circuit [75].

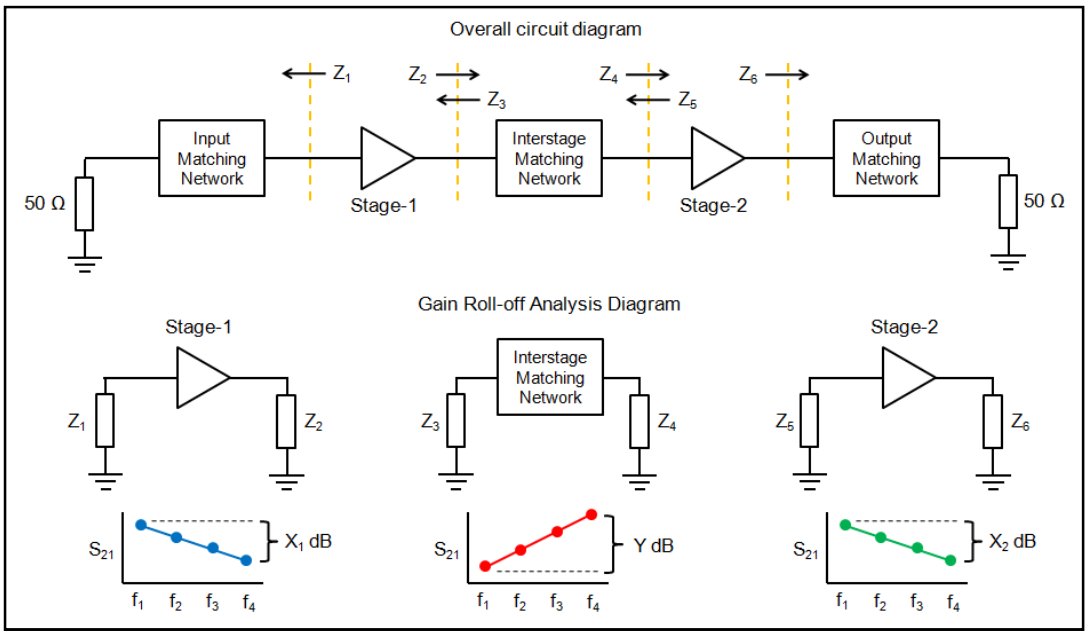


Figure 3.8 Gain Roll-Off Analysis Diagram

Figure 3.9 shows the schematic diagram of the M-probe used with ADS which is adapted from the S-probe tool [77].

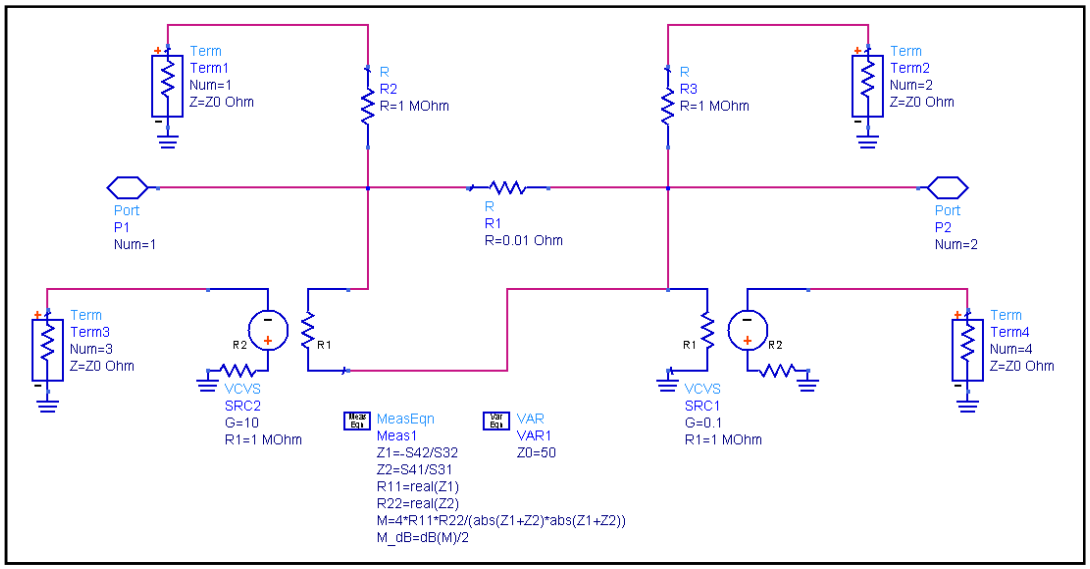


Figure 3.9 Schematic Diagram of M-Probe for implementation in ADS

The M-probe calculates the mismatch factor, *M*, and *M_dB* is the total mismatch loss between two complex impedances in dB. M-probe is placed between

stage-1 amplifier and the interstage matching network to calculate the amount of interstage mismatch loss as shown in Figure 3.10.

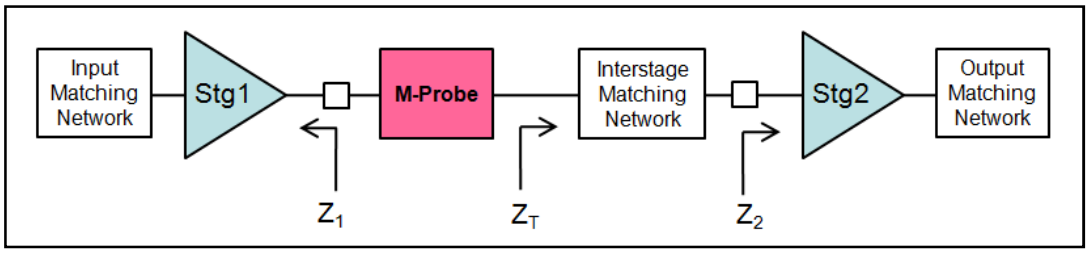


Figure 3.10 M-Probe to Calculate Interstage Mismatch Loss

Inserting M-probe using ADS into the interstage of DTN2 design with ideal components gives the mismatch loss and is tabulated in Table 3.2. The circuit was designed with higher mismatch loss at lower frequency as the gain of the amplifier tends to roll off with increasing frequency. Therefore, the gain roll-off from stage-1 and stage-2 are compensated by the mismatch factor. This example shows that the difference between interstage mismatch loss at the lowest and highest frequency is about 3 dB.

Table 3.2 Mismatch Factor for DTN2 Design

Frequency	Mismatch Loss (dB)
200 MHz	5.320
300 MHz	4.902
400 MHz	3.705
500 MHz	3.374
700 MHz	2.304

3.1.4 DC Biasing

DC Biasing is required to operate the two-stage amplifier and the switching network.

3.1.4.1 Biasing Power Amplifier

There are 4 bias voltages applied to the 2-stage power amplifier; stage-1 input bias, stage-1 output bias, stage-2 input bias and stage-2 output bias. For the Amp_A and Amp_B, both stage-1 and stage-2 input bias lines are tied together. Current divider rule is used to control the current passing through stage-1 and stage-2 input bias. DC supply is connected to series inductor or RF choke (8.2 – 68 nH) and large bypass capacitor (10 pF – 1 μF) to ensure that there is no RF signal on the DC path.

3.1.4.2 Driving and Controlling SP4T Switch

The switching function in the discrete design was implemented using Surface Mount Device 4-way switch (Skyworks SP4T AS204-80LF). The SP4T switch requires a supply voltage (V_{CC}) of $\pm$ 5 V and typical supply current of 500 μA. Combination of control voltages (CTL1 and CTL2) to control the switch is shown in Table 3.3 (Appendix A), with 2.4 – 5 V to control state "1" and 0 – 0.5 V to control state "0".

Table 3.3 Truth Table for SP4T Control Voltage

Path J1 to:	**Control Input**	
	CTL1	**CTL2**
J2	0	0
J3	1	0
J4	0	1
J5	1	1

3.1.4.3 Biasing MMIC Switching Network

In the MMIC design, 3 – 5 control FETs are integrated within the tuning elements and each FET requires a single control voltage to change the FET state. FET is turned ON when 0 V or 2 V is applied and turned off when -2 V is applied. When driving FETs, the current value must be limited. Therefore, large resistors (2 – 8 kΩ) are placed in series with the gates to protect FETs from overflowing current. The diagrams of DC biasing for the control voltage for all variants are available in the Appendix G – DC Biasing Diagram.

3.2 Stability Analysis

Particular attention was given to the amplifier stability while designing DC bias at power amplifier. *K*-factor and Δ analysis were performed individually on each amplifier stage to ensure unconditional stability. Both amplifier stages satisfy Rollet's stability conditions where $K > 1$ and $|\Delta| < 1$ for each tuner switch state and for all frequencies from about DC to operating f_T [73].

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}||S_{21}|^2} \tag{3.1}$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \tag{3.2}$$

In the design process using ADS, the *K* and Δ values can be shown as stability circles plotted on the Smith chart. The stability circles are very convenient for practical design.

3.3 Layout Design

For the discrete design, the components were placed on the prototype board as close as possible to the MMIC die. For MMIC design, after the circuit schematic was designed, the components were placed on the available die area. In this study, the die size provided were 1200 μm × 600 μm for the PD 50-01 process and 600 μm × 600 μm for the PD 50-10 process. The details are discussed in Section 3.3.1 and 3.3.2.

3.3.1 Discrete Layout Design

The layout for discrete design was done at the same time with the layout of PCB board (TN_Prototype1). The size of components are 0402 (1.0 mm × 0.5 mm) and 0805 (2.0 mm × 1.25 mm) as shown in Figure 3.11. These surface-mount devices were placed as close as possible to the amplifier to minimize parasitic effects

but still provide reasonable space for manual board component population process. The complete layout for the Discrete design can be found in Appendix F – Board Population Diagram.

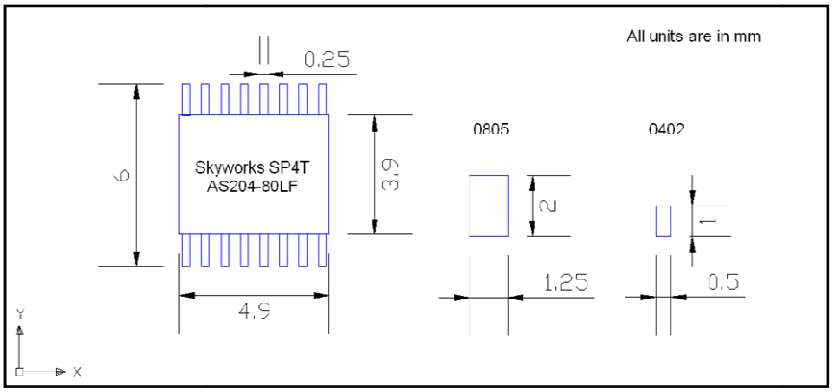


Figure 3.11 Sizes of Surface-mount Devices

3.3.2 MMIC Layout Design

Several issues must be considered in MMIC design layouts and are discussed in this section. The process used for the MMIC design was the WIN PD50-01 (ED2) 0.5 µm InGaAs pHEMT Enhancement/Depletion-Mode. For the final optimized version, the process used was WIN PD50-10 (ED3) 0.5 µm InGaAs pHEMT Enhancement/Depletion-Mode.

DC analysis is very critical for layout design especially to determine the minimum line widths necessary that connects components. Both processes have 2 – 3 metal layers and each metal has different current density limit. For example, Metal-1 has current density limit of 4 mA/µm. If the expected current passing through the line is 38 mA, the width of Metal-1 line should be at least 10 µm which provide maximum current density limit of 40 mA. The metal lines should not be too thin and long because it will introduce additional resistive loss.

Placement of components and lines should not be too close to each other to minimize electromagnetic coupling. Coupling between components might alter the circuit response but the schematic model is not able to include these effects in simulation. However, all components together with the metal lines and bondpads must fit inside a specified scribe area.

Bondpads are placed at the edge of the die to ease wirebonding process. The bondpad position must be chosen so that the wirebonds do not cross over and create possibilities of short circuit between the gold wires.

After the design layout is complete, an LVS (Layout versus Schematic) check is performed to make certain that all connections are correct according to schematic design. Then, the layout file is sent for DRC (Design Rule Check) to ensure all layers comply with the layout guidelines.

3.4 Sensitivity Analysis

For Discrete design, sensitivity analysis was only performed on variation of line dimensions on the prototype boards to estimate the worst case variation in performance. Whereas for MMIC design, sensitivity analysis was performed not only on the prototype board lines but also the variations on MMIC component dimensions. During the prototype board fabrication process, up to 10 % variation in the line width and length can be introduced. These variations were modeled using ADS Monte Carlo simulator (Figure 3.12) with a uniform distribution and 10 iterations to predict these effects. These variations were simulated and the S-parameter responses are shown superimposed on each case in Section 3.4.1, 3.4.2 and 3.4.3.

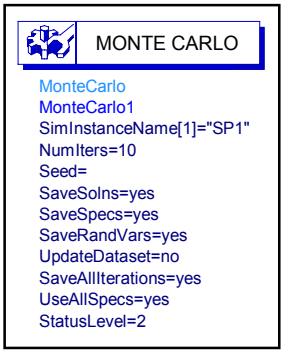


Figure 3.12 ADS Monte Carlo Simulator

3.4.1 Variation of Line Length on Prototype Board

The effects of variation of the longest RF signal lines on prototype board were simulated. These lines include the RF lines that have high possibility to introduce parasitic effects in the network. The variations of DC bias line lengths were not included in the sensitivity analysis. The maximum line length on the prototype board is about 7 mm and variation of up to ± 15 % of the total lengths were analyzed. Figure 3.13 shows the effects of board line length variations. The effects of line length variations result in little change in S_{21}, S_{11} and S_{22} (maximum variation of ± 0.15 dB).

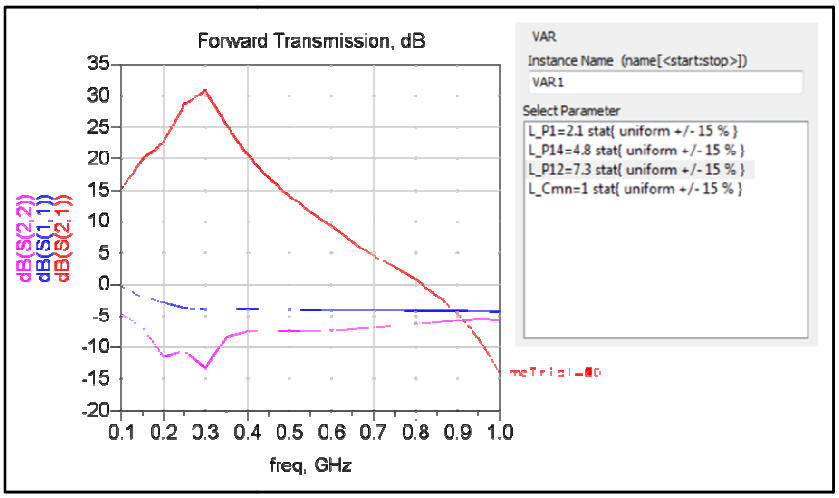


Figure 3.13 Sensitivity Analysis on Prototype Board Line Length Variations

3.4.2 Variation of Line Widths on Prototype Board

The 50 Ω microstrip line used in prototype boards has line width equal to 0.61 mm. These lines were varied by ± 10 % and simulated. In Figure 3.14, it is shown that the effects of varying board line widths result in very little changes in S_{21}, S_{11} and S_{22} (maximum variation of ± 0.1 dB).

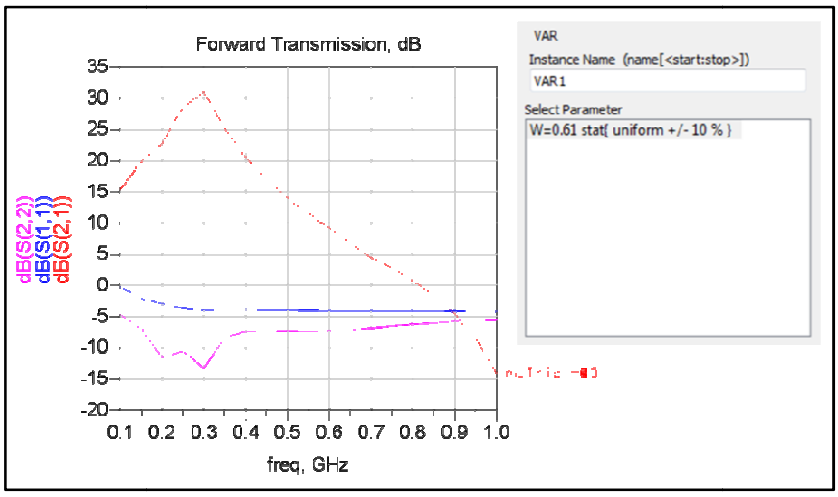


Figure 3.14 Sensitivity Analysis on Prototype Board Line Width Variations

3.4.3 Variation on MMIC Components Widths and Lengths

Sensitivity analysis was performed on the widths and lengths of MMIC capacitors with very small sizes since its impedance value is rapidly increased as increasing frequency. The length and width of several MIM and STACK capacitors were varied uniformly by up to 10 % and the S-parameters response of that variation is shown in Figure 3.15. It is shown that the S_{21} changes by $\pm$ 0.5 dB, while S_{11} and S_{22} changes very little. The variation on the MMIC components dimensions were performed up to frequency 4 GHz.

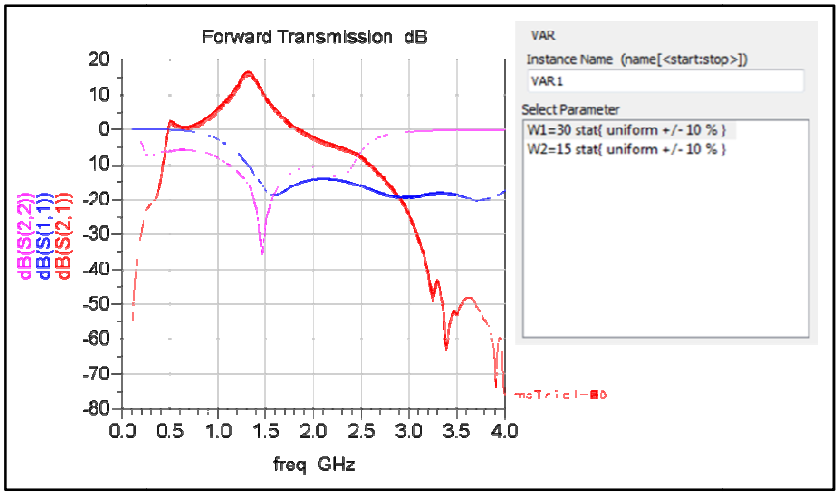


Figure 3.15 Sensitivity Analysis on MMIC layout

The sensitivity analysis was performed in all design variants for each operating state to ensure optimized result. As shown in Figure 3.13 – Figure 3.15, the simulated variations have little effects on S-parameter responses.

3.5 Prototype Board Design and Modeling

In order to reduce the cost of fabricating different prototype boards, a single board design must accommodate several design variants. Two types of boards named TN_Prototype1 and TN_Prototype2 were designed, modeled and fabricated to implement the Discrete design and MMIC design, respectively.

3.5.1 Specification of Prototype Board

The specifications of the prototype boards are:

1. Number of layers : 3
2. Dimension : 40mm (width) × 50mm (length)
3. Material : Roger4350 10mil + FR4 0.5/0.5
4. Finished Thickness : 52mils ± 4mils (TN_Prototype1)
   42mils ± 4mils (TN_Prototype2)
5. Finishing : Immersion Gold/ S/MASK & CNC ROUTED

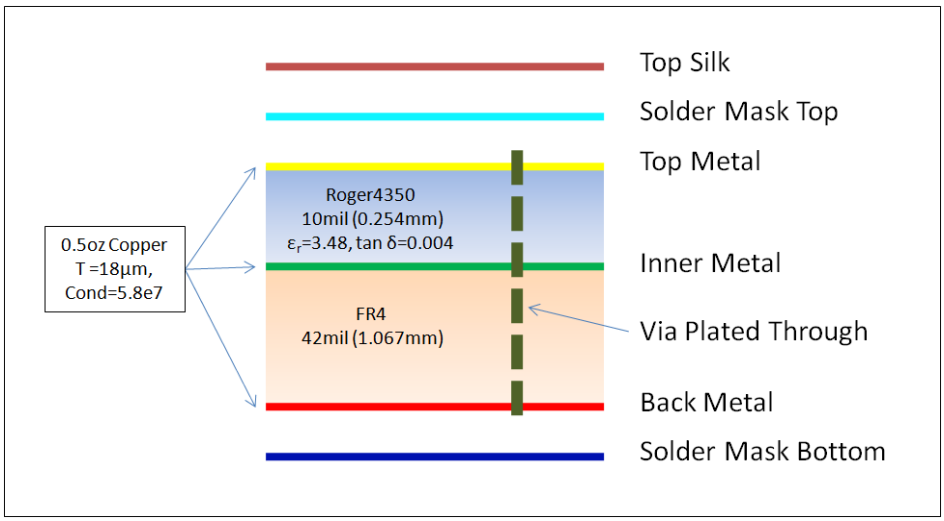


Figure 3.16 Cross Section of Prototype Board

The board layers are shown in Figure 3.16. The layers are defined as:

1. Top Silk : top layer white printing for text.
2. Solder Mask Top : green layer solder mask protecting top metal.
3. Top Metal : top metal layer.
4. Inner Metal : metal at middle layer that acts as RF ground.
5. Back Metal : bottom metal layer.
6. Solder Mask Bottom : green layer solder mask protecting bottom metal.
7. Via Plated Through : via hole connects the top metal to other metal layer.

Top and bottom metal are only exposed at certain places with gold finishing for wire-bonding and soldering purposes. Half ounce copper (Cu) with 18µm thickness is used for all three metal layer. Gold finishing is sputtered on top of nickel (Ni) layer which is adhesive to copper (Cu) as shown in Figure 3.17.

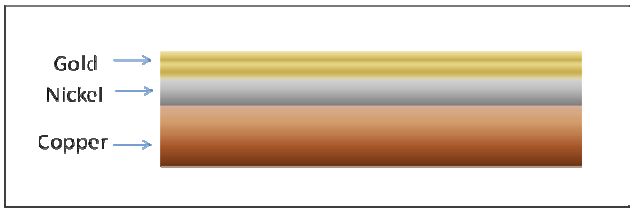


Figure 3.17 Metal Exposure with Flash Gold Finishing

The substrate used between top metal and inner metal is Roger 4350 with 10 mil thickness, dielectric constant (ε_r) of 3.48, and loss tangent ($tan\delta$) of 0.004. Between the inner metal and back metal, FR4 is used as the support layer with 42 mil or 32mil thickness, dielectric constant (ε_r) of 4.5, and loss tangent ($tan\delta$) of 0.001. The thickness of substrates was designed to fit the gap between the connector's legs as shown in Figure 3.18.

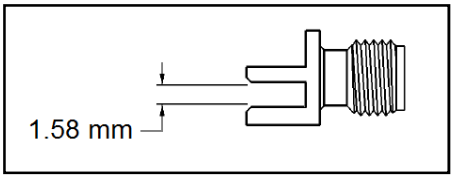


Figure 3.18 SMA Connector Dimension

3.5.2 Layout of Prototype Board

Initially, layout design of prototype board was done using AutoCAD 2007. The layout was imported to Agilent's Advanced Design System 2008 which was then converted to Gerber file (standard file format for PCB fabrication). Complete figure of prototype board is provided on Appendix B.

Since inner metal acts as RF ground, via connecting top/back metal to the inner metal is a ground connection as shown in Figure 3.19. Connection from top metal to back metal has to be done using via without touching inner metal layer as shown in Figure 3.19.

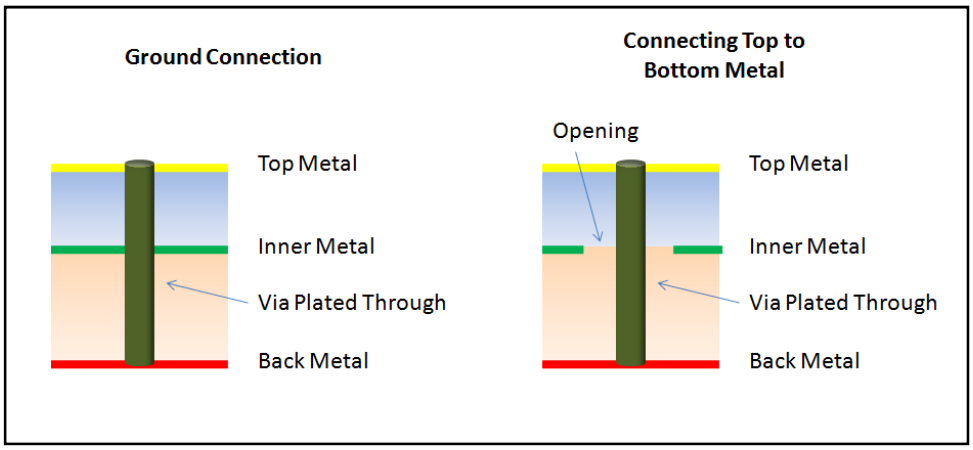


Figure 3.19 Layer Connections on Prototype Board

3.6 Electromagnetic Simulation

Sonnet™ software was used to perform full-wave EM analysis to include the parasitics from prototype board into the circuit simulation. The top metal is the layer with the most complex structure. Therefore, only the top metal layer was simulated to reduce the memory requirement of the simulation. The EM simulations were performed at frequency between 0.1 GHz to 4 GHz with 0.1 GHz steps. The field simulation was drawn with cell size 0.1 mm × 0.1 mm in a box size of 60 × 70 cells as shown in Figure 3.20.

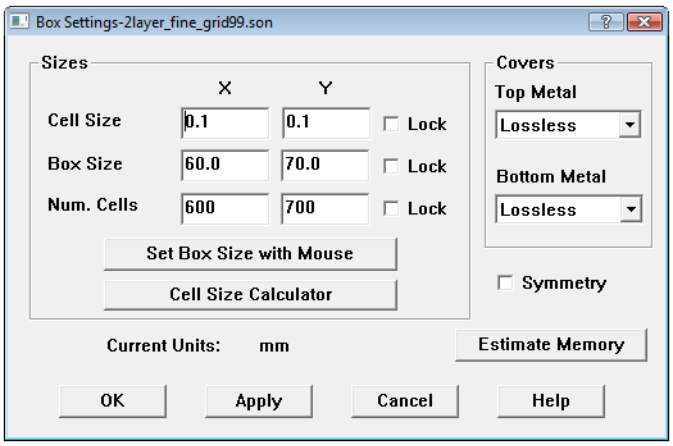


Figure 3.20 Box Setting for Prototype Board in Sonnet™ Software

Ground connections were included using square vias as shown in Figure 3.21. The simulation also includes the characteristics of Roger substrate as well as the copper layer (thickness and conductivity). Even though field simulator is highly accurate, it is not preferred in design tasks as it takes very long to compute the responses. The EM simulation for the prototype board takes about 36 – 48 hours.

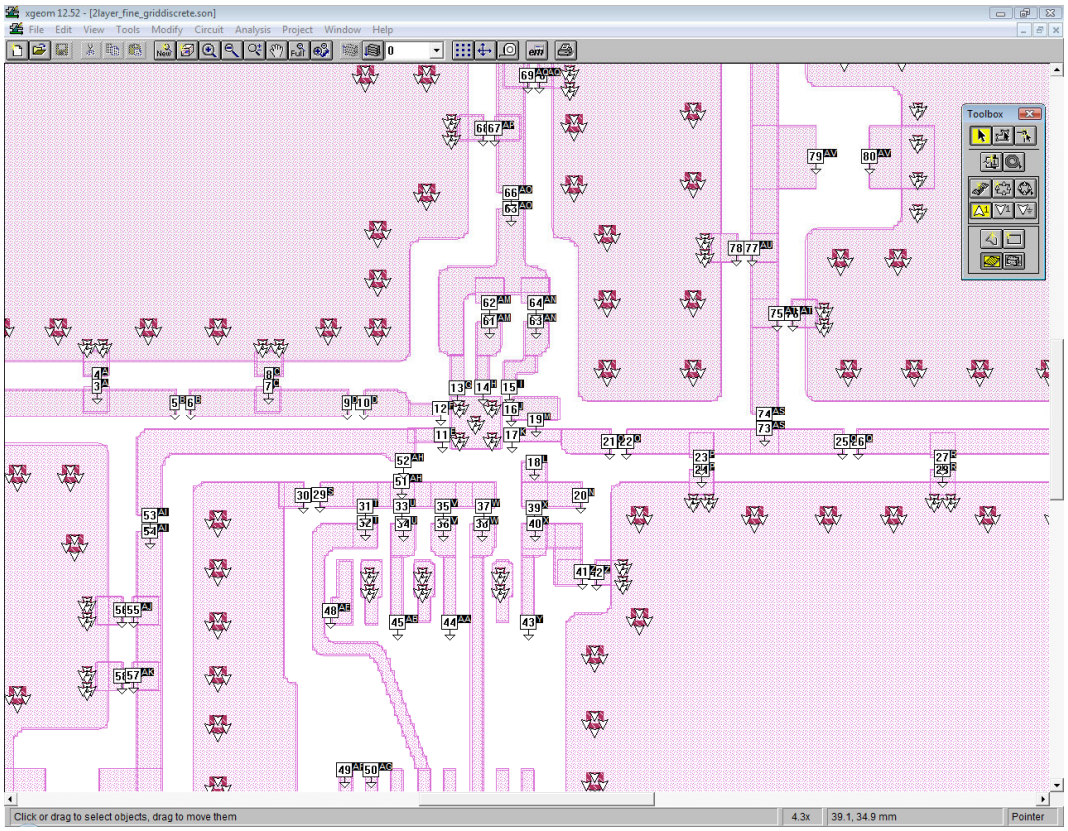


Figure 3.21 Snapshot of TN_Prototype1 Layout in Sonnet™ Software

Standard ports and co-calibrated ports were included in the simulation so that the Touchstone data produced by field simulator can be integrated in the schematic simulation. There are 81 co-calibrated ports (internal ports) included in TN_Prototype1 simulation and 97 co-calibrated ports (internal ports) included in TN_Prototype2. The layout of the prototype boards with the ports are shown in Figure 3.22. The more detailed diagrams for the EM-simulated prototype board and port numbers can be found in Appendix H – Prototype Board Layout on EM-Simulator.

Figure 3.23 shows the hybrid EM-circuit simulation for variant TO0. The Touchstone data from prototype board's EM-simulation was integrated in the ADS schematic simulation using Data File tool. The other parasitic effects that are not accounted in the S-parameter block, such as wirebonds, bondpads and vias between top metal to bottom metal, are included using the ADS model.

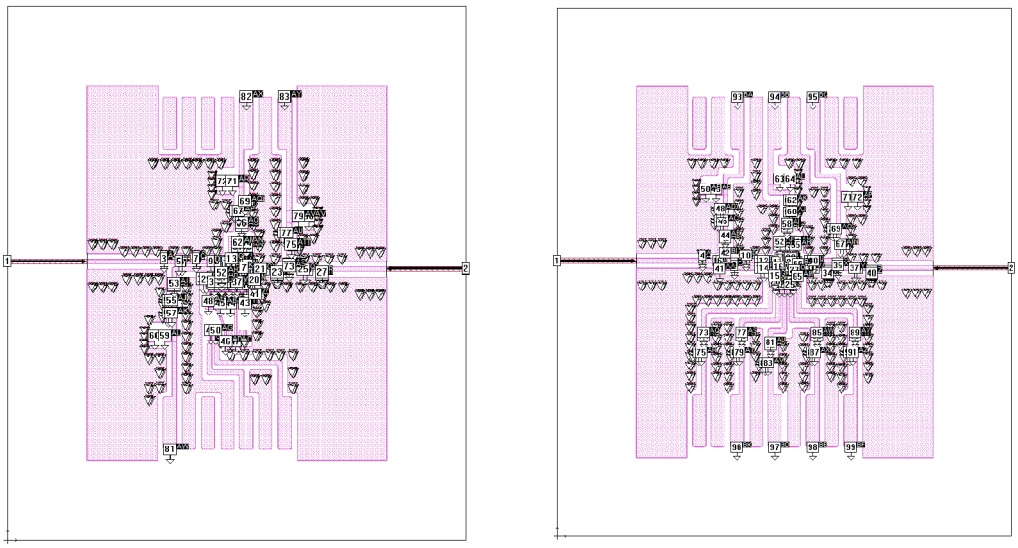


Figure 3.22 TN_Prototype1 and TN_Prototype2 Layout in Sonnet^{TM} Software

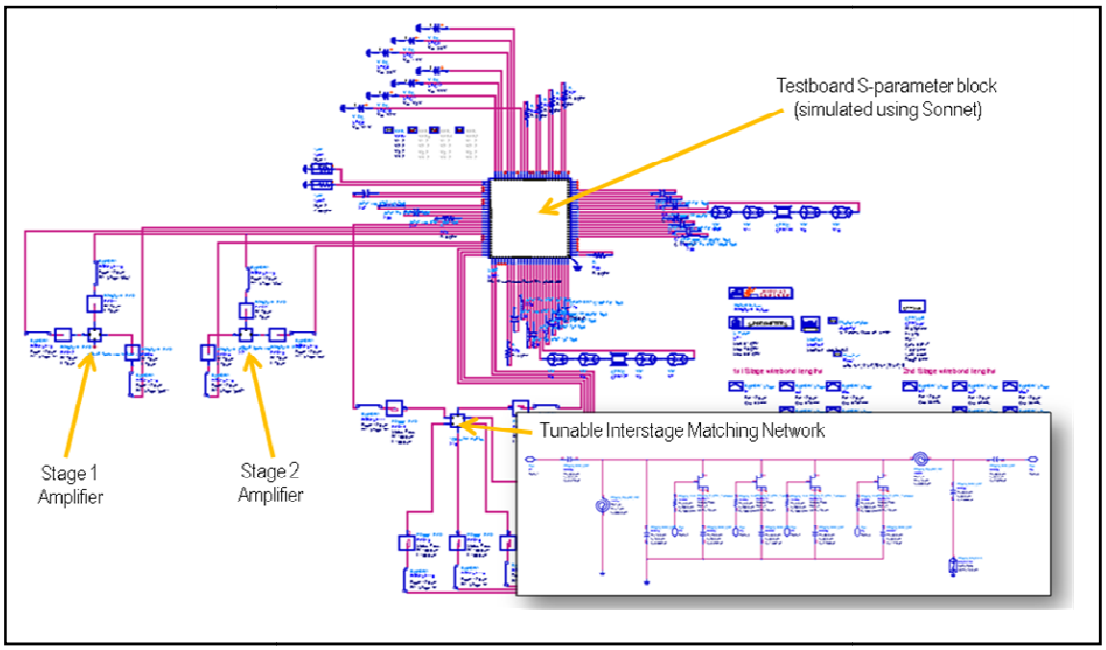


Figure 3.23 Hybrid EM-Circuit Simulation for Reconfigurable PA (TO0)

3.7 Fabrication

Experimental setup and fabrication process were performed in three sessions. The first session was intended for Discrete design and the other two were done for MMIC design and its final optimized version.

3.7.1 MMIC Fabrication

The die tape out was done by WIN Semiconductor and takes 8 weeks to fabricate. This fabrication process produces around 4 – 5 samples for each variant. Figure 3.24 shows the fabricated dies on a gel container.

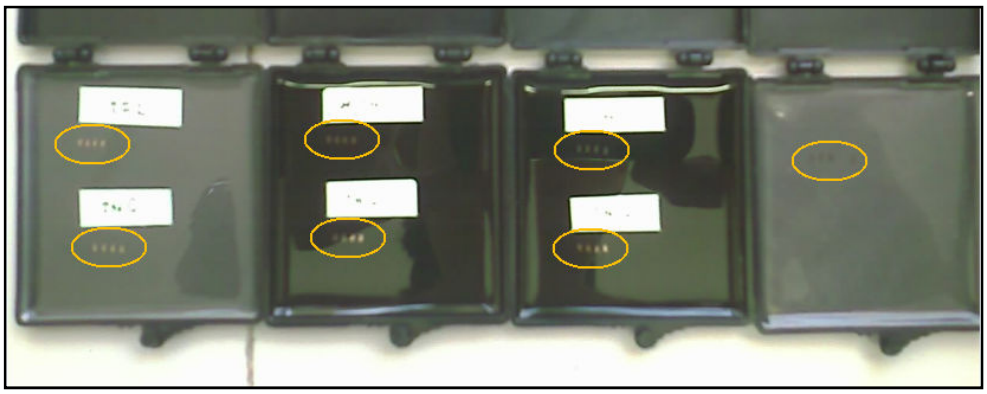


Figure 3.24 Fabricated Dies on Gel Container

3.7.2 Die Attach

Each die is attached using conductive epoxy (Diemat) onto its position on the prototype board. This process has to be done under the microscope of at least 10 times magnification to ensure that no epoxy is scattered and create short circuit to ground. Next, during the curing process, the boards were placed inside an oven with the temperature set to ramp up to ± 175˚C within 30 minutes. Then, the boards were left in the oven for another 50 minutes. Figure 3.25 shows the Diemat epoxy, curing process and the attached dies.

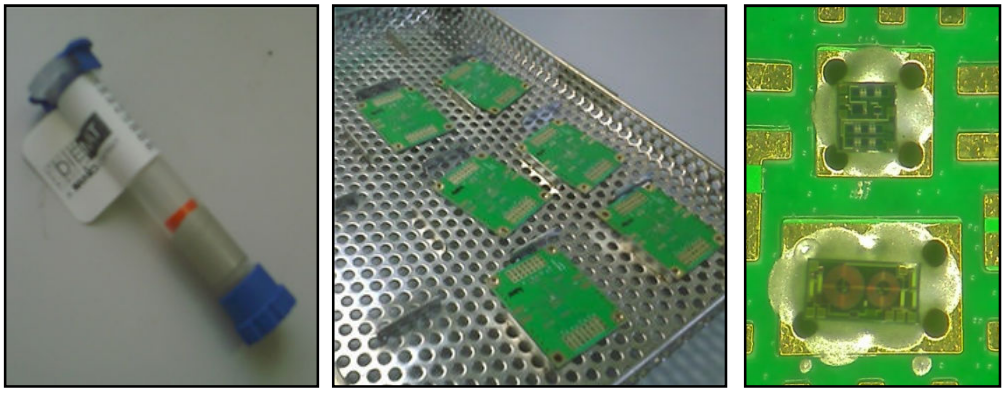


Figure 3.25 Diemat epoxy, curing process and attached dies on prototype board

3.7.3 Board Population

The board population is the most time consuming process as it is done manually using microscope, two sets of very fine tipped solder and solder paste dispenser as shown in Figure 3.26.

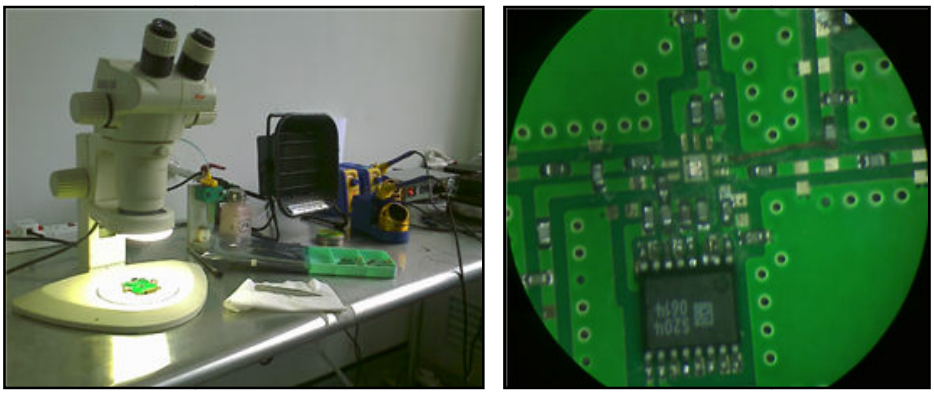


Figure 3.26 Soldering Station and Populated Board

For the Discrete design, before soldering the SP4T, its pin has to be altered by keeping pin #3 hanging and creating a solder bridge from pin #2 to #3 in order to connect the grounds as shown in Figure 3.27.

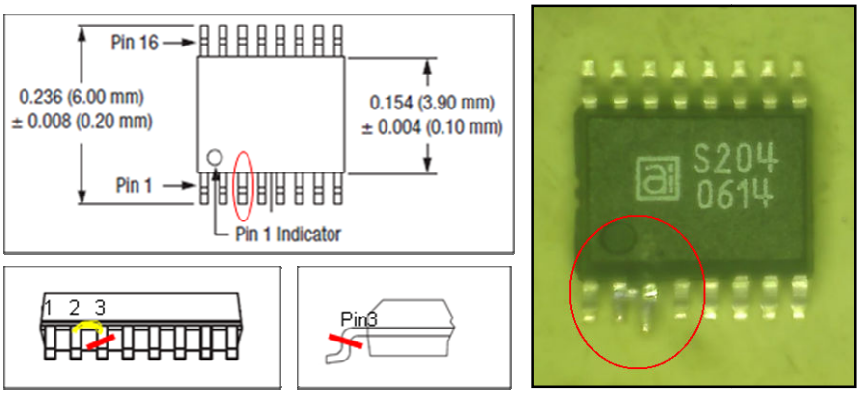


Figure 3.27 Alter pins of Skyworks SP4T AS204-80LF

The SP4T switch and other 0402 and 0805 components are then soldered onto their places according to Board Population diagram in Appendix F. For MMIC design, the number of surface-mount components is limited to input/output matching networks and biasing network hence simplify the board populating process.

Next step is to install the SMA connectors at input and output then setup DC pins and their twisted cables connection to the DC supply.

3.7.4 Wire Bond

The wire bond machine used was a semi-automatic K&S 4524AD machine. The bonding technique was ball – wedge using 1 mil gold wire. The smallest bondpad size is 75 µm × 75 µm. Figure 3.28 shows the wirebonded dies located on a prototype board.

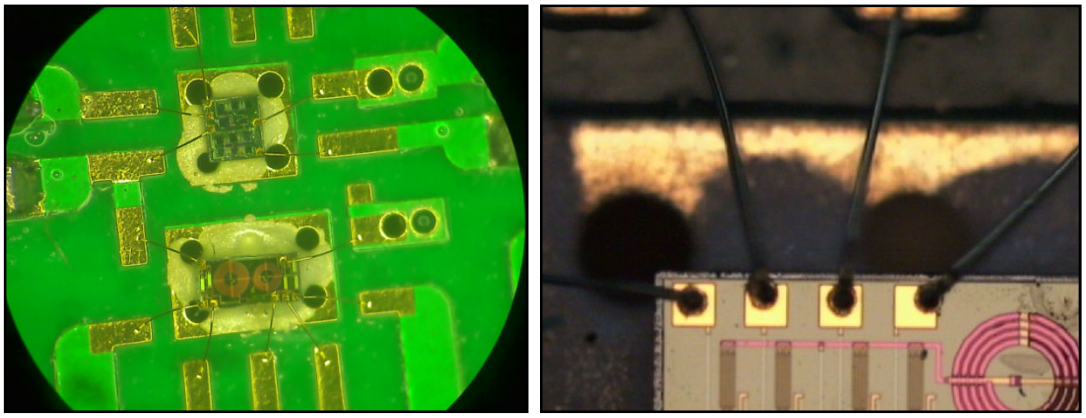


Figure 3.28 Wirebonded Dies and 1 mil Gold Wire

3.8 Measurements

This section discusses the measurement setup for small signal and large signal measurement.

3.8.1 Small Signal Measurement

The diagram illustrated in Figure 3.29 shows the equipment setup used to measure S-parameters of the fabricated boards. The model of Network Analyzer is Agilent E5071C 9kHz – 8.5 GHz (ENA Series Network Analyzer) and the model of DC power supply is the Agilent E3631A (Triple Output DC Power Supply).

The input and output of Device Under Testing (DUT) are connected to port 1 and port 2 of Network Analyzer, respectively. The DC power supplies are connected to DC pins for biasing the power amplifier and also for the switching network. The diagram showing voltage and current limit applied on the circuit is available in Appendix G – DC Biasing Diagram. A calibration has to be done prior to S-parameter measurement using either manual calibration kit or electronic calibration kit. The S-parameter data was saved in Touchstone format (sNp) that can be plotted together with the simulated data in ADS.

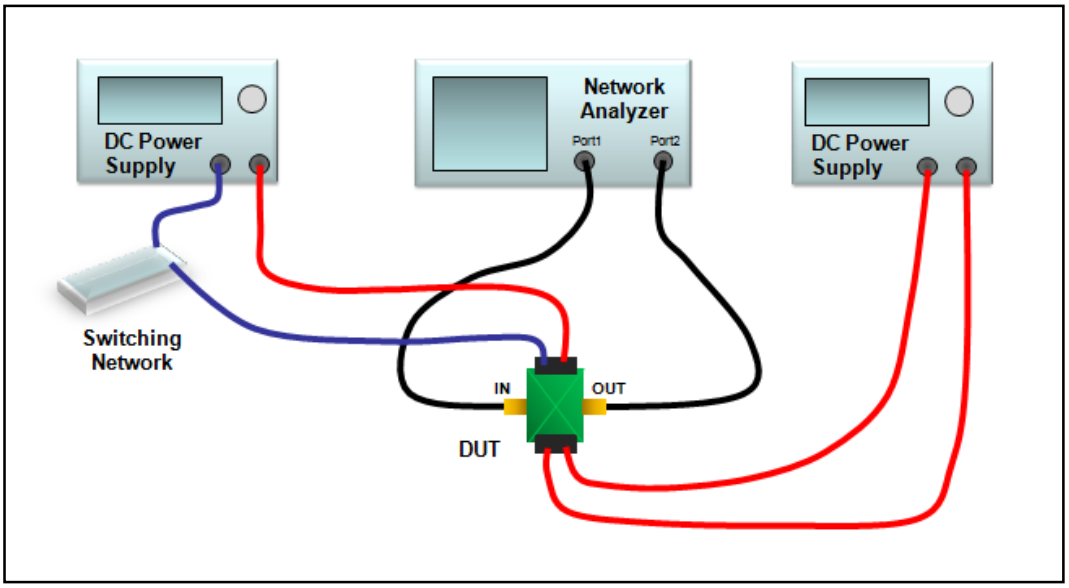


Figure 3.29 Equipment Setup for S-Parameter Measurement

3.8.2 Large Signal Measurement

The illustration shown in Figure 3.30 shows the equipment setup for P_{1dB} measurement. The model of Spectrum Analyzer is Agilent MXA N9020A 20 – 26.5 GHz and the model of Analog Signal Generator is Agilent MXG N5181A 100 kHz – 6 GHz.

The Signal Generator generates signal at certain frequency and power which is fed into the input of DUT. This signal is then amplified by the reconfigurable power amplifier and its output goes to spectrum analyzer. Attenuator of 40 dBm is placed before the spectrum analyzer to protect the spectrum analyzer. The value of

output power at specified frequency can be read at the spectrum analyzer. These values and the cable losses were then documented in spreadsheet and computed to determine the correct P_{1dB} of the circuit.

DC power supplies are connected to DC pins for power amplifier biasing and also for the switching network.

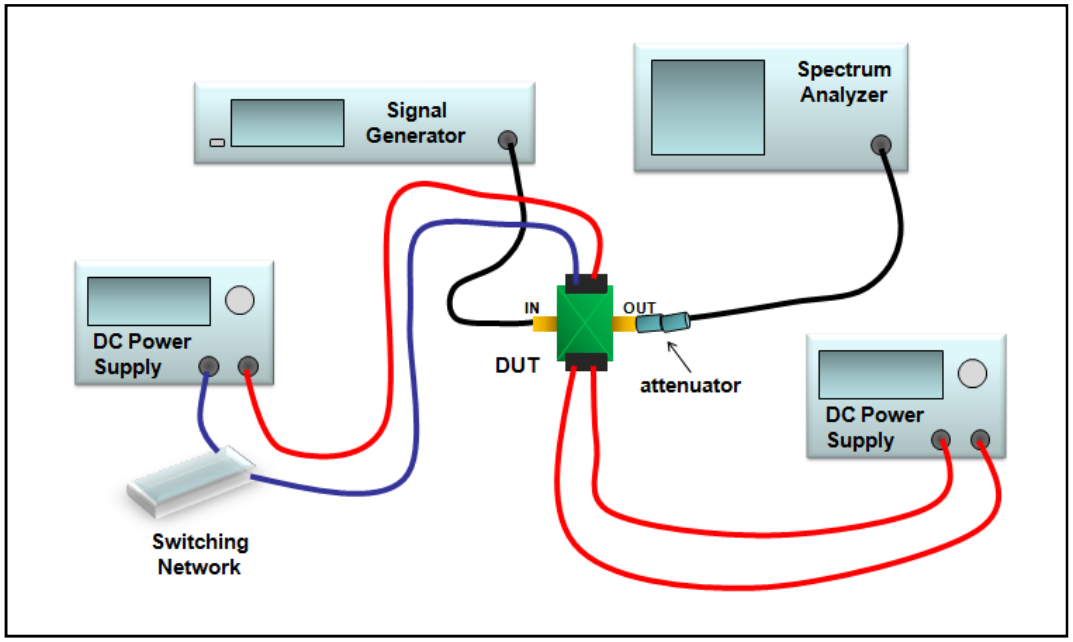


Figure 3.30 Equipment Setup for P_{1dB} Measurement

The illustration in Figure 3.31 shows the equipment setup for OIP3 measurement. Two signal generators, each is set at +/- 5 kHz difference from the operating frequency with the same power level, generate analog signals which are combined together by a power combiner. The output of power combiner is fed into the input of DUT. This signal is then amplified by the reconfigurable power amplifier and its output goes to spectrum analyzer. Attenuator of 40 dBm is placed before the spectrum analyzer to protect the device. An isolator was included before each signal generator to prevent interaction between signal generator #1 and #2. At spectrum analyzer, the output power at first and second harmonics can be seen on the screen and then the data were tabulated and computed together with cable losses to obtain the correct OIP3 values.

DC power supplies are connected to DC pins for power amplifier biasing and also for the switching network. The two signal generators and spectrum analyzer has to be tied together at the back side to synchronize the clock time of these devices.

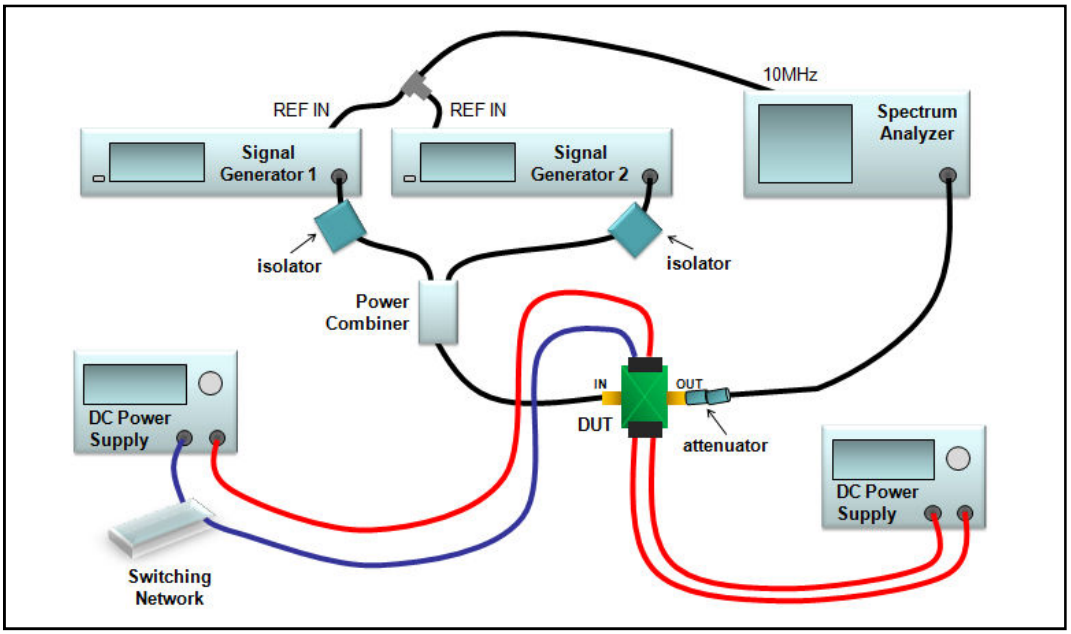


Figure 3.31 Equipment Setup for OIP3 Measurement

3.9 Design Variants

This section shows the designed and fabricated variants of Discrete design in Table 3.4 and MMIC design in Table 3.5.

Table 3.4 Design Description of Discrete Tunable Interstage Matching Network

Design ID	Topology	Description
DTN1	T-section	Tunable inter-stage matching network for Amp_A
DTN2	T-section	Tunable inter-stage matching network for Amp_B
DTN3	Π-section	Tunable inter-stage matching network for Amp_B

All variants in Table 3.5 were fabricated on GaAs MMIC dies. However, not all of them were able to be populated on prototype board and measured due to time and resource limitation.

Table 3.5 Design Description of MMIC Tunable Interstage Matching Network

ID	Process	Size (x by y)	Description
TN0	ED2	600×1200 μm	• Tunable interstage matching network for Amp_A • π–network • Freq: 1.18, 1.54, 1.87,2.37 GHz
TN1	ED2	600×1200 μm	• Tunable interstage matching network for Amp_A • T–network • Freq: 0.89, 1.61, 1.87, 2.38 GHz
TN2	ED2	600×1200 μm	• Tunable interstage matching network for Amp_B • T–network • Freq:0.91, 1.57, 1.90, 2.44 GHz
TN3	ED2	600×600 μm	• Tunable interstage matching network for Amp_B • π–network • Freq: 0.90, 1.58, 1.80 GHz
TF1	ED2	600×600 μm	• Tunable Filter using 3 FET switches • LC-network • Freq: 0.85 – 1.85 GHz
TF2	ED2	600×1200 μm	• Tunable Filter using 4 FET switches • LC-network • Freq: 0.89 – 2.40 GHz
TO0	ED3	2 dies @ 600×600 μm	• Tunable interstage matching network for Amp_A • optimized • Freq: 1.32 – 2.03 GHz
TO1	ED3	600×600 μm	• Tunable interstage matching network for Amp_A • optimized • Freq: 0.87 – 1.08 GHz

Chapter 3 discusses systematically the steps taken to realize the prototype of reconfigurable power amplifier using interstage matching network. There are 2 main design configurations in prototype realization: 1) discrete design and 2) GaAs MMIC design.

This chapter discusses the circuit design methodology that includes initial design, Smith chart method and exploitation of interstage mismatch loss. It is followed by stability analysis to ensure unconditional stability. The layout design step is where two design configurations slightly differ as the discrete components were positioned on the prototype board itself while the MMIC designs were fabricated on GaAs wafer space. The discussion in sensitivity analysis, prototype board modelling, electromagnetic simulation and fabrication process can also be found in this chapter. This chapter also shows diagrams and explanation of small signal and large measurement setup. The last section of this chapter lists the design variants for both discrete and GaAs MMIC designs in tables.

CHAPTER 4

RESULTS AND DISCUSSIONS

The prototypes for the reconfigurable power amplifier were realized using two different design configurations. Both configurations use 2-stage MMIC power amplifiers and the interstage matching networks used in this chapter are as follows:

1. Discrete Design: Interstage matching network using surface-mount components.
   (Variants: DTN1, DTN2 and DTN3)
2. Quasi-MMIC Design: Interstage matching network using separate GaAs MMIC die.
   (Variants: TN2, TN31 and TO0)

Two to five prototype boards were fabricated for each design variant. The details for each board setup are available in Appendix E – G.

In this chapter, the detailed schematic for each variant including the DC biasing network to operate the circuit are presented and discussed. The simulated and measured small signal and large signal data are shown and compared in graphs and tables.

4.1 TN_Prototype1 (Discrete Design)

Three variants of reconfigurable power amplifier using discrete interstage matching network are discussed in this section. Figure 4.1 shows the fabricated prototype board for the discrete design.

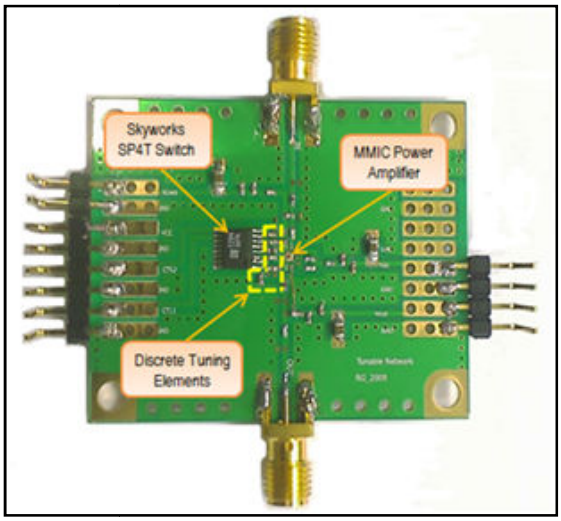


Figure 4.1 Photo of prototype board with MMIC PA and discrete tuning elements

4.1.1 DTN1 with Amp_A (T-section)

DTN1 is a tunable interstage matching network designed to complement the two-stage amplifier Amp_A. The reconfigurable power amplifier was designed to operate at frequency between 0.9 GHz to 2.2 GHz and realized using MMIC power amplifier and discrete components.

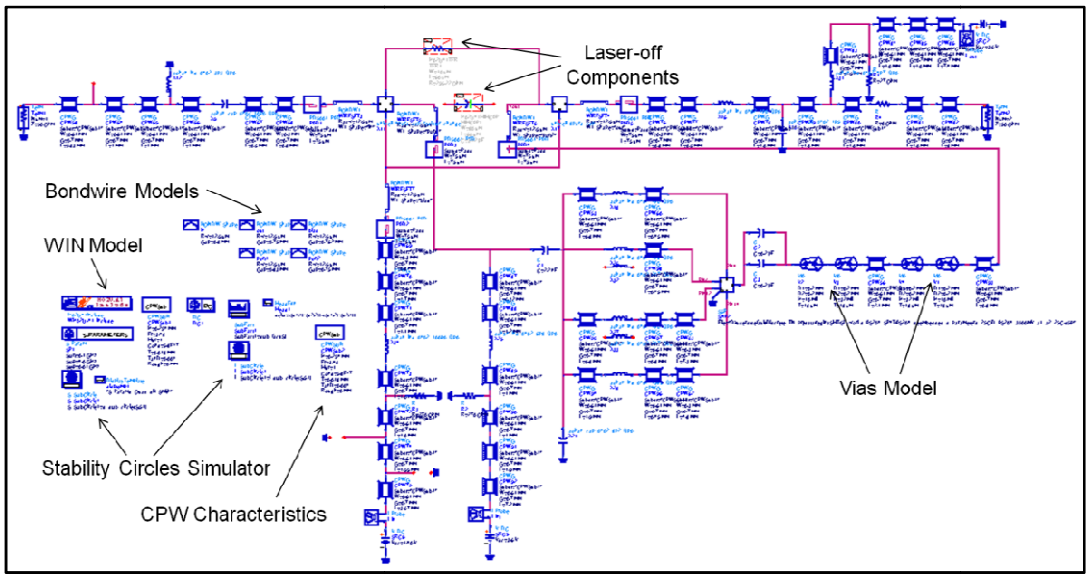


Figure 4.2 ADS Simulation for DTN1

The first step was the initial circuit designs that include the ballasting and biasing network for the two-stage amplifier and wideband matching networks using highpass L-section in the input and lowpass L-section in the output as elaborated in Section 3.1.1. A comprehensive stability analysis was also performed for each amplifier stage and at each tuning states to ensure unconditional stability. The circuit simulation and stability analysis were performed using ADS software. The parasitic from the prototype board were accounted into the simulation using the CPW model in ADS as shown in Figure 4.2.

The T-section topology used in the interstage consists of series inductors, a shunt capacitor and a series capacitor that forms a bandpass structure. The inductance value is switched using a discrete SP4T switch between 4 different inductor values. The values of components in the input and output networks were tuned along the process of interstage network design to ensure good return loss.

A schematic diagram of the reconfigurable power amplifier using DTN1 tunable interstage matching network is shown in Figure 4.3. To operate the amplifier with variant DTN1, the following bias voltages are applied: 1) Input bias $V_{in} = 1.4\ V$ $(I_{in} = 6.92\ mA)$, 2) Output1 bias $V_{out1} = 3.6\ V$ $(I_{out1} = 48.60\ mA)$, and 3) Output2 bias $V_{out2} = 3.6\ V$ $(I_{out2} = 235.3\ mA)$. Supply voltage $(V_{CC} = 5\ V,\ I_{CC} = 0.5\ mA)$ is required to turn on the SP4T switch. The SP4T control voltage required are 2 V for state "1" and 0 V for state "0".

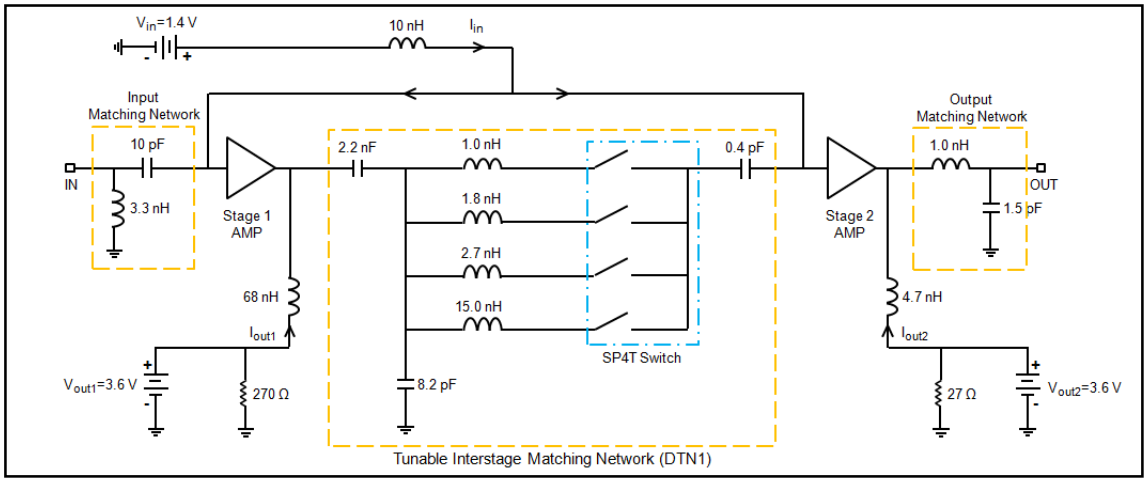


Figure 4.3 Schematic Diagram of Reconfigurable PA with DTN1 Interstage Matching Network

Table 4.1 shows binary combinations of control voltages (CTL 1 and CTL 2) for DTN1 and the corresponding operating frequencies.

Table 4.1 Binary combinations of SP4T control voltage for DTN1

CTL 1	CTL 2	Series Inductor	Operating Frequency (f_o)
0	0	15.0 nH	660 MHz
1	0	2.7 nH	1.370 GHz
0	1	1.8 nH	1.500 GHz
1	1	1.0 nH	1.610 GHz

Figure 4.4 shows both measured and simulated S_{21}, S_{11}, and S_{22} at four different center frequencies. The solid lines indicate measured data and dotted lines indicate the simulated data.

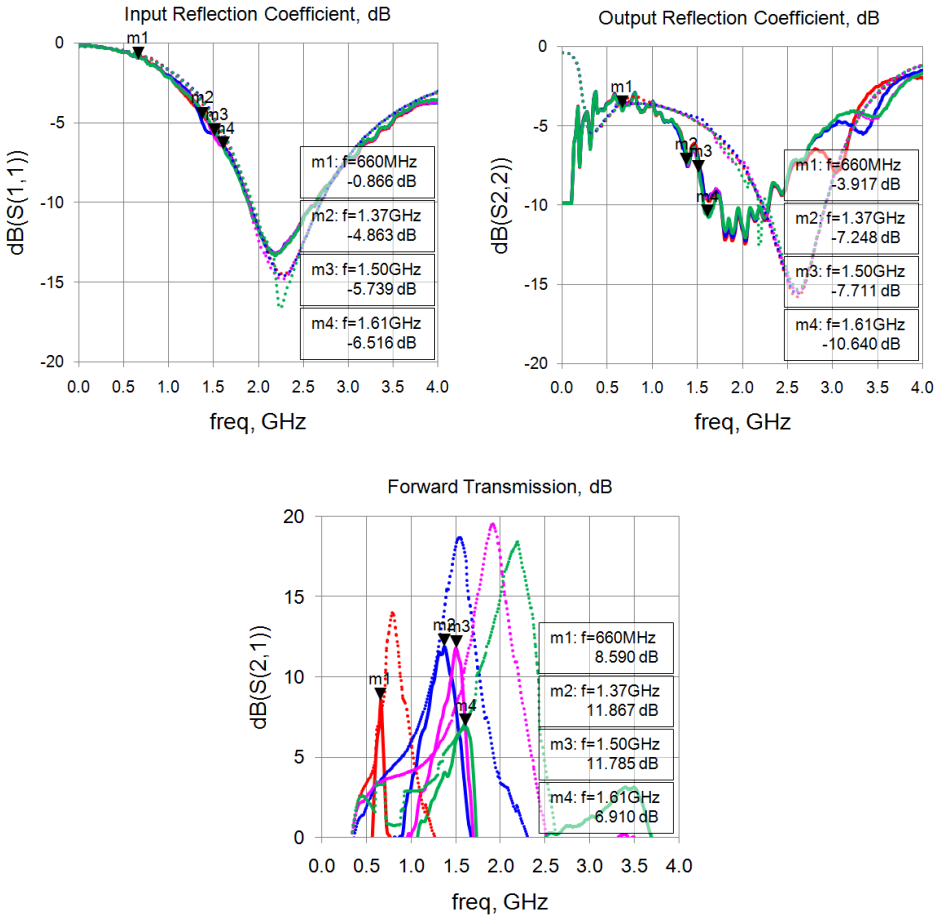


Figure 4.4 Measured Vs. Simulated S-Parameters for DTN1

The measured gain for DTN1 prototype varies from 7 dB to 12 dB. It does not agree with the simulated data very well as shown in Figure 4.3. The reconfigurable PA with interstage matching network has the following operating frequencies; 660 MHz, 1.370 GHz, 1.500 GHz, and 1.610 GHz. The measured input reflection coefficient (S_{11}) varies from -1 dB to -5 dB. The output reflection coefficient (S_{22}) varies from -4 dB to -10 dB at the operating frequencies. The minimum reverse isolation (S_{12}) is -45 dB. The simulated and measured center frequencies, the corresponding bandwidth and Q-factor are shown in Table 4.2.

Table 4.3 shows the simulated and measured operating frequencies (f_o) and the 3-dB bandwidth.

Table 4.2 3-dB Bandwidth at varying operating frequencies for DTN1

Simulated f_o	790 MHz	1.540 GHz	1.920 GHz	2.190 GHz
Simulated 3-dB BW	160 MHz	220 MHz	230 MHz	300 MHz
Measured f_o	660 MHz	1.370 GHz	1.500 GHz	1.610 GHz
Measured 3-dB BW	90 MHz	270 MHz	180 MHz	280 MHz

Because of the complex layout of the prototype board, the effects of these parasitic at higher frequencies cannot be properly accounted using the ADS models. To predict the circuit responses more accurately, the prototype board was modeled using a full-wave electromagnetic analysis program Sonnet^{TM}. The electromagnetic (EM) analysis includes the prototype board's parasitic effects from the coupling between adjacent microstrip lines and the distributed inductances and capacitances of the microstrip lines.

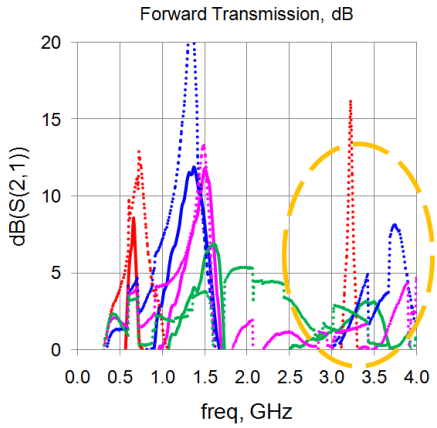


Figure 4.5 Measured Vs. Partial-EM Simulated S-Parameters for DTN1

Sonnet™ was used to simulate electromagnetic coupling of the prototype board as described in Section 3.6. The generated SnP block was included in the hybrid EM-circuit simulation. The hybrid-EM simulation predicts the measured response more accurately as shown in Figure 4.5. The unwanted gain at higher frequency indicated by the circle is due to parasitic effects from the prototype boards. Low frequency operations experience less parasitic effects due to the nature of distributed inductance and capacitance that form a low-pass structure. For instance, the variant DTN2 and DTN3 are designed for lower operating frequencies (f_o < 1 GHz) and the simulation responses give reasonable agreement even without EM-simulated prototype board model (refer to section 4.1.2 and 4.1.3).

Table 4.3 shows the simulated and measured gain compression (P_{1dB}) and linearity (OIP3) for DTN1.

Table 4.3 Measured P_{1dB} and OIP3 of Reconfigurable MMIC PA for DTN1

Operating Freq (f_o)	660 MHz	1.370 GHz	1.500 GHz	1.610 GHz
Simulated P_{1dB} (dBm)	12.771	15.329	14.589	11.429
Measured P_{1dB} (dBm)	14.02	16.73	16.09	11.61
Simulated OIP3 (dBm)	23.314	25.867	25.242	21.256
Measured OIP3 (dBm)	25.01	27.995	27.00	23.63

4.1.2 DTN2 with Amp_B (T-section)

DTN2 is a tunable interstage matching network designed to complement the two-stage amplifier Amp_B. The previous design shows that discrete components cannot be used to realize reconfigurable power amplifier for high frequency operation. This variant was designed to operate at lower frequency band (f_0 < 1 GHz) and realized using MMIC power amplifier and discrete components.

After biasing Amp_B, stabilizing Amp_B and placing series capacitance in the input and output matching network, the graphical method using Smith chart was used to determine the interstage topology. The T-section topology used in the interstage matching network consists of a large series inductor (L_1), shunt capacitor (C_2) and series capacitor (C_1). This structure transforms the impedance Z_2 to a higher impedance value and intersects the high Q-factor lines to achieve narrow bandwidth (Z_2 to A'). The shunt capacitor transforms the impedance at point A' to B'. The series capacitor transforms the impedance from B' to Z_T for each operating frequency. The impedance transformations for 5 different operating frequencies are shown in Figure 4.6.

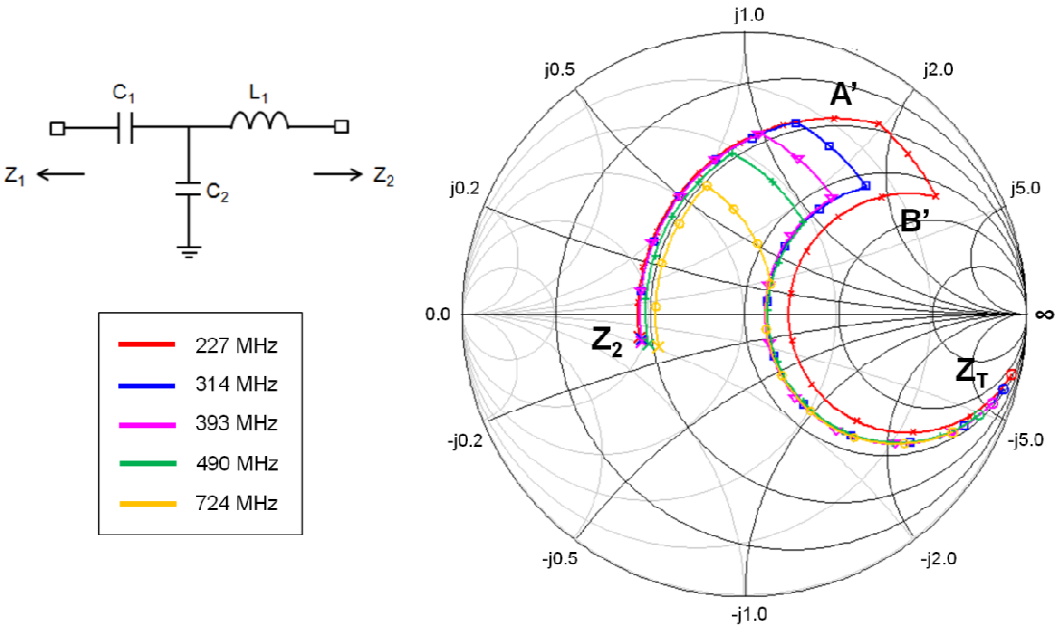


Figure 4.6 T-section impedance transformation at different states for DTN2

The next step is to analyze the gain roll-off at each stage of amplifier Amp_B by simulating each stage separately. The gain drop between the lowest and highest operating frequency is 2.119 dB in stage-1 and 2.611 dB in stage-2 as shown in Figure 4.7. The total gain drop across the tuning bandwidth is 4.730 dB.

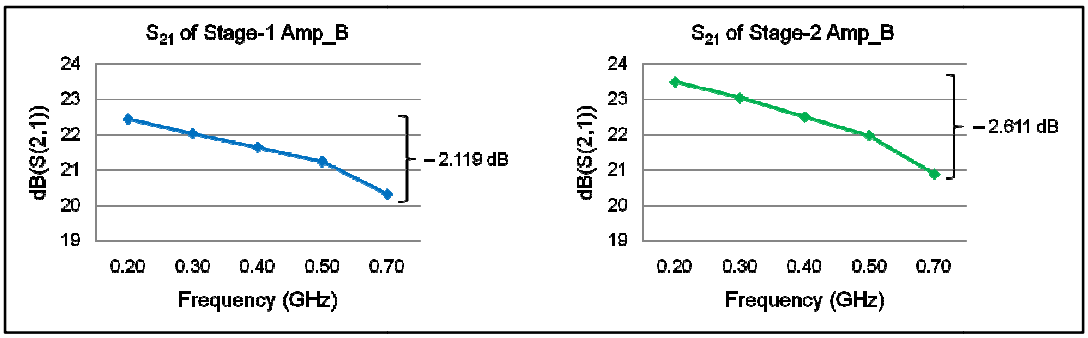


Figure 4.7 Gain Roll-off Analysis for Amp_B

Table 4.4 Interstage Mismatch Loss for DTN2

Operating Freq (f_o)	Mismatch Loss
227 MHz	5.962 dB
314 MHz	4.628 dB
393 MHz	3.792 dB
490 MHz	3.428 dB
724 MHz	2.386 dB

Ideally, Z_2 should be transformed to Z_1* to obtain maximum power transfer. However, the difference between the transformed impedance (Z_T) and Z_1* results in interstage mismatch loss. Table 4.4 shows the mismatch loss at Z_1 (between output impedance of first stage amplifier and the interstage) and at Z_2 (between the interstage and input impedance of second stage amplifier). In this design, the difference between interstage mismatch loss at the highest and lowest operating frequency is only 3.576 dB. The interstage mismatch loss was not optimized to compensate for the total gain drop across the tuning bandwidth resulting in a gain variation of about 2 dB for different tuning states.

A schematic diagram of reconfigurable power amplifier using DTN2 tunable interstage matching network is shown in Figure 4.8. To operate the amplifier with variant DTN2, the following bias voltages are applied: 1) Input bias V_{in} = 5 V (I_{in} =

15.28 mA), 2) Output1 bias V_{out1} = *5 V* (I_{out1} = *73.27 mA)*, and 3) Output2 bias V_{out2} = *5 V* (I_{out2} = *161.4 mA)*. Supply voltage (V_{CC} = *5 V*, I_{CC} = *0.5 mA*) is required to turn on the SP4T switch. The SP4T control voltage required were 2 V for state "1" and 0 V for state "0". Table 4.5 shows binary combinations of control voltages (CTL 1 and CTL 2) for DTN2 and the corresponding operating frequencies.

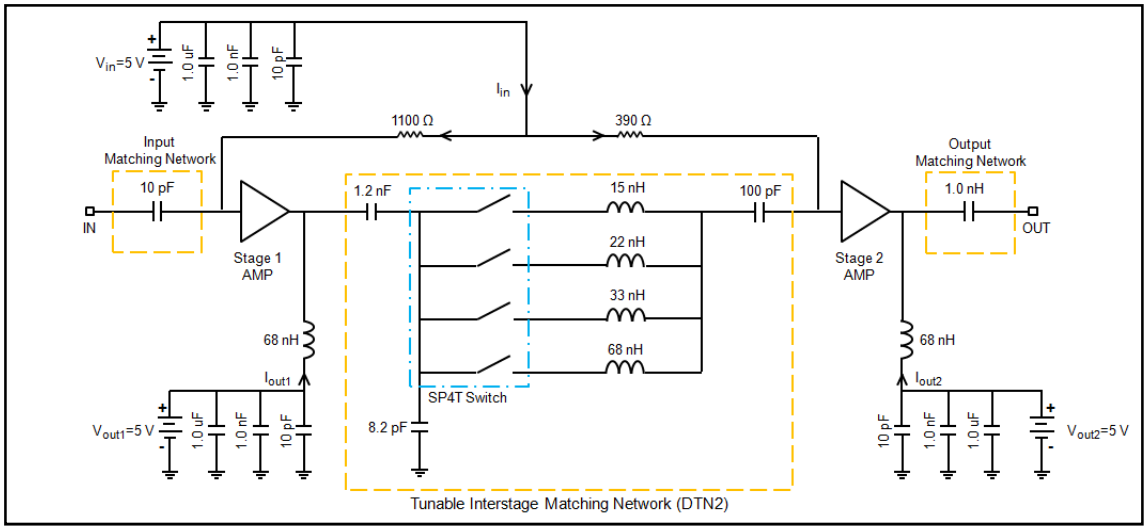


Figure 4.8 Schematic Diagram of Reconfigurable PA with DTN2 Interstage Matching Network

Table 4.5 Binary combinations of SP4T control voltage for DTN2

CTL 1	CTL 2	Series Inductor	Operating Frequency (f_o)
0	0	68.0 nH	227 MHz
1	0	33.0 nH	314 MHz
0	1	22.0 nH	393 MHz
1	1	15.0 nH / 8.2 nH	490 MHz / 724 MHz

Figure 4.9 shows both measured and simulated S_{21}, S_{11}, and S_{22} at five different center frequencies. The solid lines indicate measured data, the dotted lines indicate the circuit-simulated data and the thin dashed lines indicate the hybrid EM-circuit data. The fabricated DTN2 prototype provides an average of 34.5 dB (± 2.0 dB) gain which gives reasonable agreement with the simulated data. The reconfigurable PA with interstage matching network operates at 227 MHz, 314 MHz, 393 MHz, 490 MHz, and 724 MHz (if inductor 15 nH is replaced by 8.2 nH).

The input reflection coefficient (S_{11}) provides -5 dB at all operating frequencies. Output reflection coefficient (S_{22}) is less than -10 dB for each state. The minimum of reverse isolation (S_{12}) is -45 dB for all states.

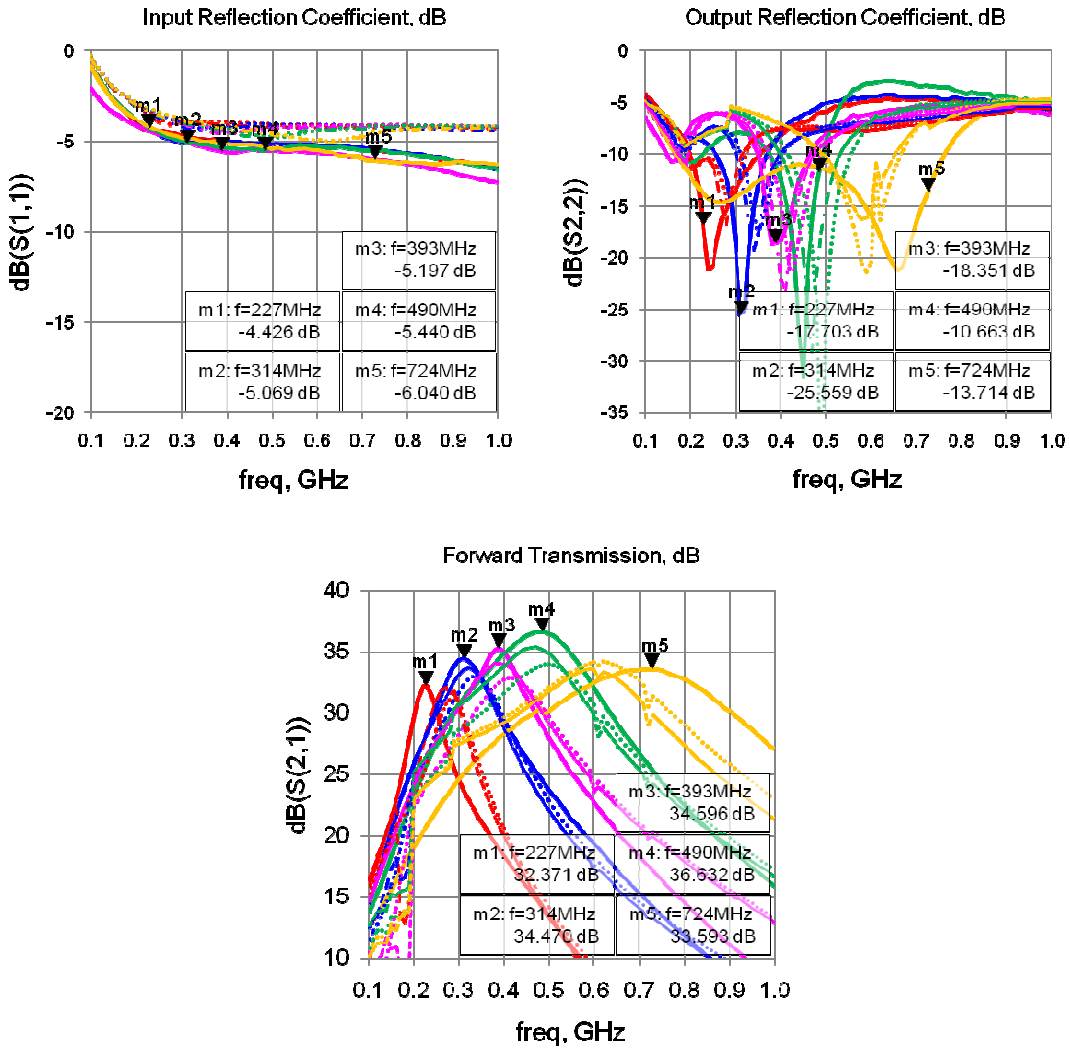


Figure 4.9 Measured Vs. Simulated S-Parameters for DTN2

Table 4.6 shows the simulated and measured operating frequencies (f_o), the corresponding bandwidth, and the Q-factor ($Q = f_o / BW_{3dB}$). Matching-Q is the highest Q-contour value that was achieved in the initial design using graphical Smith chart method. For the DTN2 design with T-section topology, the measured 3-dB Q value is nearly the same as the matching-Q.

Table 4.6 3-dB Bandwidth at varying operating frequencies for DTN2

Simulated f_o	288 MHz	338 MHz	414 MHz	500 MHz	616 MHz
Simulated 3-dB BW	68 MHz	120 MHz	167 MHz	213 MHz	270 MHz
Measured f_o	227 MHz	314 MHz	393 MHz	490 MHz	724 MHz
Measured 3-dB BW	570 MHz	110 MHz	103 MHz	205 MHz	370 MHz

Table 4.7 shows the amount of gain rejection for operating frequency. For example, when state 1 operates (f_o = 227 GHz), the gain rejection at the adjacent operating frequency (314 GHz) is 8.552 dB. Table 4.8 shows the simulated and measured gain compression (P_{1dB}) and linearity (OIP3) for DTN2.

Table 4.7 Measured Gain Rejection for DTN2

Operating Frequency	**Gain Rejection (dB) at**				
	227 MHz	314 MHz	393 MHz	490 MHz	724 MHz
227 MHz		8.552	13.506	18.616	32.319
314 MHz	5.945		4.444	10.270	19.888
393 MHz	8.312	3.481		5.986	17.042
490 MHz	10.686	5.477	2.214		10.834
724 MHz	12.689	8.605	5.589	3.706	

Table 4.8 Measured P_{1dB} and OIP3 of Reconfigurable MMIC PA for DTN2

Operating Freq (f_o)	227 MHz	314 MHz	393 MHz	490 MHz	724 MHz
Simulated P_{1dB} (dBm)	19.83	19.86	20.31	21.39	22.05
Measured P_{1dB} (dBm)	22.182	23.576	23.505	23.465	23.995
Simulated OIP3 (dBm)	40.519	40.702	40.782	41.252	41.380
Measured OIP3 (dBm)	29.56	32.798	33.125	34.505	35.780

4.1.3 DTN3 with Amp_B (π-section)

DTN3 is a tunable interstage matching network designed to complement the two-stage amplifier Amp_B. DTN2 shows the feasibility of using discrete components to build the tunable interstage matching network. DTN3 variant uses π-section topology to obtain response with narrower bandwidth that operates at lower frequency band (f_0 < 1 GHz). This variant is also realized using MMIC power amplifier and discrete components.

The same amplifier as in DTN2 (Amp_B) was used in this design. The π-section topology used in the interstage matching network consists of 4 components. The shunt capacitor (C_3) transforms impedance Z_2 to *A'*, the series inductor (L_1) transforms impedance *A'* to *B'*, the shunt capacitor (C_2) transforms impedance *B'* to *C'*, and the series capacitor (C_1) transforms impedance *C'* to Z_T. This topology takes the impedance to the high Q-factor lines through a lower impedance using relatively smaller inductor values that leads to less space required. The impedance transformations for 5 different operating frequencies are shown in Figure 4.10.

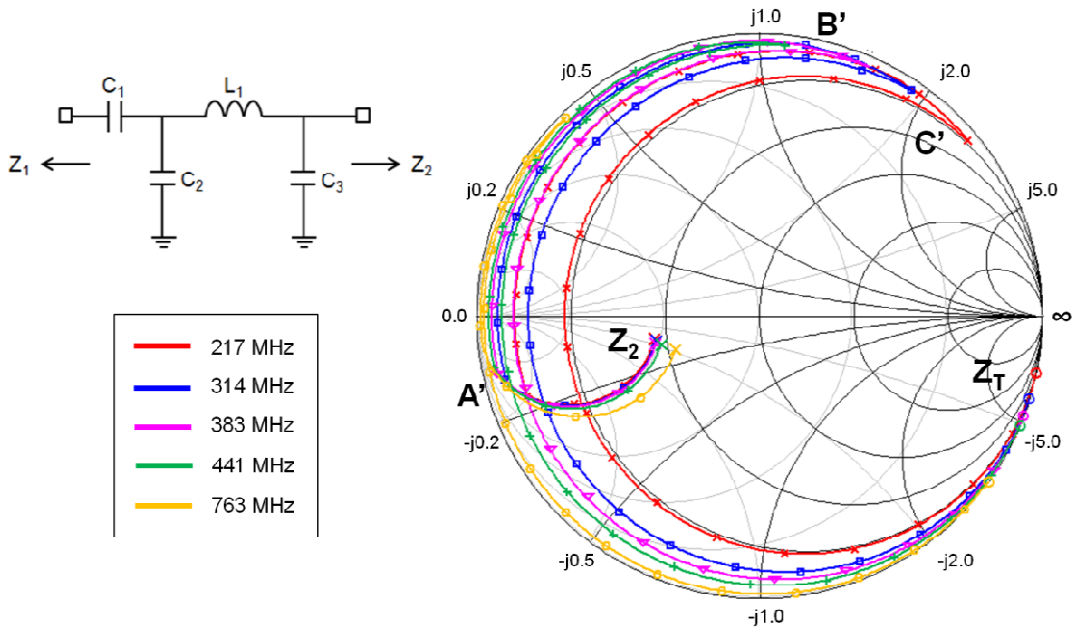


Figure 4.10 π-section impedance transformation at different states for DTN3

The gain roll off analysis for the amplifier used in this variant are shown in the previous section (Section 4.1.2).

Table 4.9 Interstage Mismatch Loss for DTN3

Operating Freq (f_o)	Mismatch Loss
217 MHz	5.563 dB
314 MHz	5.128 dB
383 MHz	4.774 dB
441 MHz	3.878 dB
763 MHz	3.591 dB

Ideally, Z_2 should be transformed to Z_1* to obtain maximum power transfer. However, the difference between the transformed impedance (Z_T) and Z_1* results in interstage mismatch loss. Table 4.9 shows the calculated mismatch loss at Z_1 (between output impedance of first stage amplifier and the interstage) and at Z_2 (between the interstage and input impedance of second stage amplifier). In this design, the difference between interstage mismatch loss at the highest and lowest operating frequency is only 1.972 dB. The interstage mismatch loss was not optimized to compensate for the total gain drop across the tuning bandwidth (4.730 dB) resulting in a gain variation of about 2.3 dB for different tuning states.

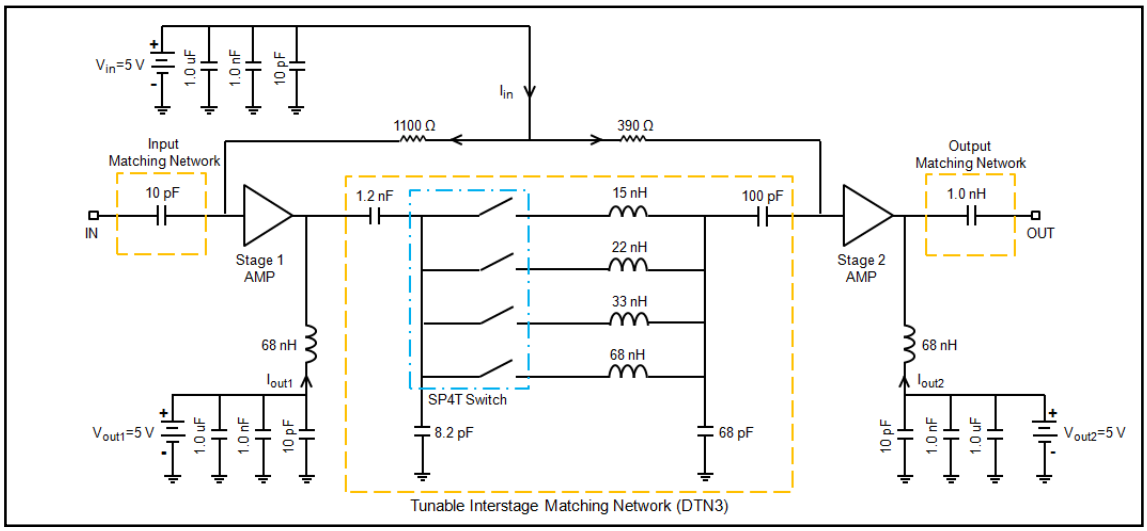


Figure 4.11 Schematic Diagram of Reconfigurable PA with DTN3 Interstage Matching Network

A schematic diagram of reconfigurable power amplifier using DTN3 tunable interstage matching network is shown in Figure 4.11. To operate the amplifier with variant DTN3, the following bias voltages are applied: 1) Input bias V_{in} = 5 V (I_{in} =

15.28 mA), 2) Output1 bias V_{out1} = *5 V* (I_{out1} = *73.27 mA)*, and 3) Output2 bias V_{out2} = *5 V* (I_{out2} = *161.4 mA)*. Supply voltage (V_{CC} = *5 V*, I_{CC} = *0.5 mA*) is required to turn on the SP4T switch. The SP4T control voltage required were 2 V for state "1" and 0 V for state "0". Table 4.10 shows binary combinations of control voltages (CTL 1 and CTL2) for DTN3 and the corresponding operating frequencies.

Table 4.10 Binary combinations of control voltage for DTN3

CTL 1	CTL 2	Series Inductor	Operating Frequency (f_o)
0	0	68.0 nH	217 MHz
1	0	33.0 nH	314 MHz
0	1	22.0 nH	383 MHz
1	1	15.0 nH / 8.2 nH	441 MHz / 763 MHz

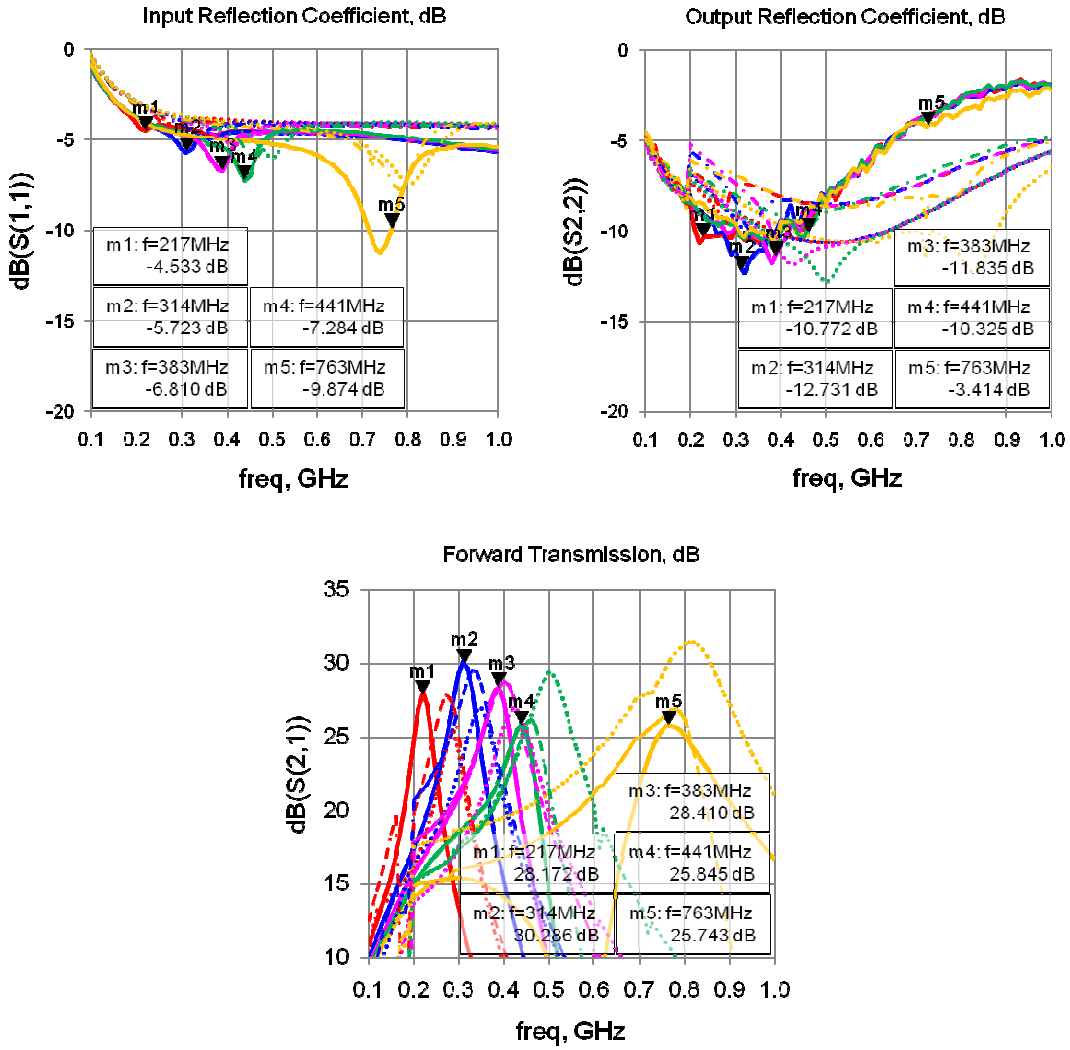


Figure 4.12 Measured Vs. Simulated S-Parameters for DTN3

Figure 4.12 show both measured and simulated S_{21}, S_{11}, and S_{22} at the five operating frequencies. The solid lines indicate measured data, the dotted lines indicate the circuit-simulated data and the thin dashed lines indicate the hybrid EM-circuit data. The fabricated DTN3 prototype provides average of 28 dB ($\pm$ 2.2 dB) gain and gives reasonable agreement with the simulated data. The reconfigurable PA with interstage matching network operates at 217 MHz, 314 MHz, 383 MHz, 441 MHz, and 763 MHz (when inductor 15 nH is replaced by 8.2 nH). The input reflection coefficient (S_{11}) varies from -4.5 dB to -10 dB at the operating frequencies. The measured and simulated output reflection coefficient (S_{22}) is less than -10 dB at nearly all state. The minimum of reverse isolation (S_{12}) is -45 dB for all states.

Figure 4.12 shows that as the frequency increases, the circuit-simulated and measured data shows more disagreement. However, the hybrid EM-circuit data indicated by the thin dashed lines can predict the measured responses more accurately even at the higher operating frequency.

Table 4.11 shows the simulated and measured operating frequencies (f_o) and the corresponding bandwidth.

Table 4.11 3-dB Bandwidth at varying operating frequencies for DTN3

Simulated f_o	290 MHz	347 MHz	424 MHz	502 MHz	813 MHz
Simulated 3-dB BW	51 MHz	67 MHz	81 MHz	84 MHz	148 MHz
Measured f_o	217 MHz	314 MHz	383 MHz	441 MHz	763 MHz
Measured 3-dB BW	37 MHz	47 MHz	58 MHz	66 MHz	141 MHz

Table 4.12 Measured Gain Rejection for DTN3

Operating Frequency	**Measured Gain Difference (dB) at**				
	217 MHz	314 MHz	383 MHz	441 MHz	763 MHz
217 MHz		16.066	25.461	29.789	28.667
314 MHz	11.302		13.731	19.761	34.106
383 MHz	11.644	6.909		8.991	44.504
441 MHz	9.972	7.050	3.747		25.383
763 MHz	11.158	10.380	11.457	12.838	

Table 4.12 shows gain rejections for each state at the operating frequencies. Table 4.13 shows the simulated and measured gain compression (P_{1dB}) and linearity (OIP3) for DTN3.

Table 4.13 Measured P_{1dB} and OIP3 of Reconfigurable MMIC PA for DTN3

Operating Freq (f_o)	217 MHz	314 MHz	383 MHz	441 MHz	763 MHz
Simulated P_{1dB} (dBm)	16.082	22.037	22.862	22.81	23.171
Measured P_{1dB} (dBm)	18.60	18.85	19.52	21.26	21.20
Simulated OIP3 (dBm)	39.134	40.635	40.572	40.309	41.651
Measured OIP3 (dBm)	28.615	32.565	34.03	33.615	34.115

For DTN2 and DTN3, the simulated and measured P_{1dB} for each operating frequency differ by 2 – 3 dB. This difference is caused by additional losses from wire bonds, connectors and RF cables that could not be included in simulation. The differences between simulated and measured OIP3 were caused not only by the additional losses but also the limitation of the models. Only a small-signal model, in Touchstone format, is available for the SP4T switch. Therefore, its large signal responses were not properly modeled.

4.2 TN_Prototype2 (Quasi-MMIC Design)

TN_Prototype2 is the prototype board designed to accommodate the Quasi-MMIC Design. Three variants (TN2, TN31 and TO0) of the reconfigurable power amplifier using GaAs MMIC interstage matching network are discussed in this section. The motivation for realizing reconfigurable power amplifier in GaAs MMIC are: 1) reduced circuit size, 2) reduced parasitic effects from discrete components, 3) flexibility to determine the exact component value and 4) enable operation at higher frequency (f_o > 1 GHz). All graphs in this section use the hybrid EM-circuit simulation data instead of the regular ADS circuit simulation data. Figure 4.13 shows the fabricated TN_Prototype2 board.

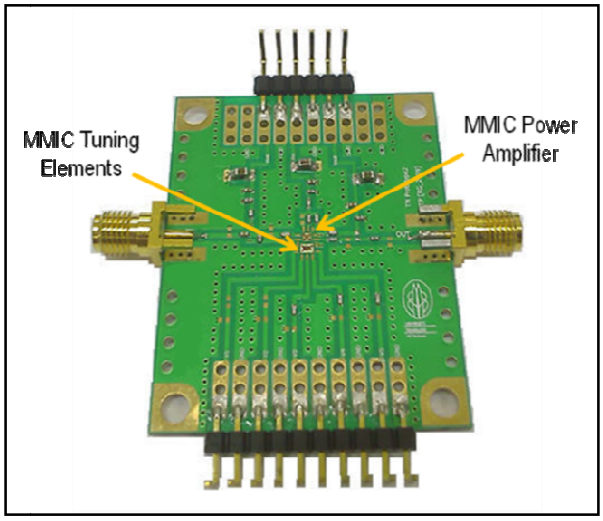


Figure 4.13 Photo of prototype board with MMIC PA and MMIC tuning elements

4.2.1 TN2 with Amp_B

TN2 is a tunable interstage matching network designed to complement the two-stage amplifier Amp_B. This variant uses series inductance and capacitors topology to obtain its responses. The total series capacitance value is varied using series FET switches. This variant is realized using MMIC power amplifier and MMIC interstage matching network.

A schematic diagram of reconfigurable power amplifier using TN2 tunable interstage matching network is shown in Figure 4.14. To operate the amplifier with

variant TN2, the following bias voltages are applied: 1) Input bias V_{in} = *5 V* (I_{in} = *15.29 mA)*, 2) Output1 bias V_{out1} = *5 V* (I_{out1} = *67.67 mA)*, and 3) Output2 bias V_{out2} = *5 V* (I_{out2} = *161.8 mA)*. The control voltages applied at gate terminal of FET switches were 0 V for on-state and -2 V for off-state. Table 4.14 shows four binary combinations of control voltages (V_1, V_2, V_3, and V_4) for TN2 and the corresponding operating frequencies. Other combinations of control voltages result in one of the aforementioned operating frequencies or slightly different.

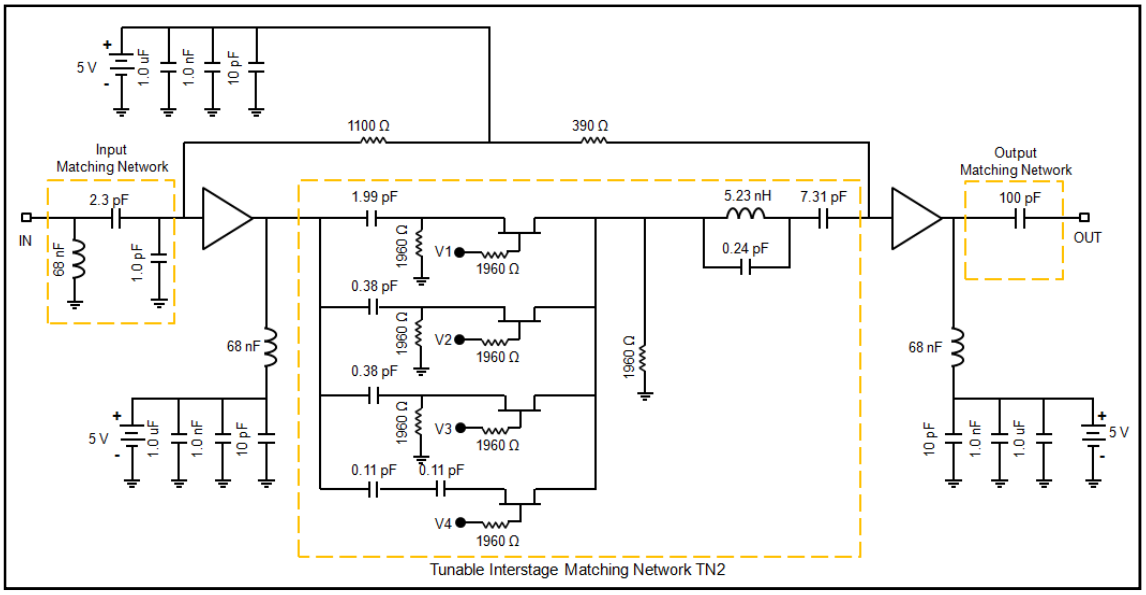


Figure 4.14 Schematic Diagram of Reconfigurable PA with TN2 Interstage Matching Network

Table 4.14 Binary combinations of FET states for TN2

FET 1	FET 2	FET 3	FET 4	Overall Capacitance	Operating Frequency (f_o)
on	on	on	on	2.805 pF	760 MHz
on	off	off	on	2.045 pF	800 MHz
off	on	on	on	0.815 pF	1.260 GHz
off	off	off	off	0.159 pF	1.420 GHz

Figure 4.15 shows the photo of fabricated TN2 die co-located with the two-stage amplifier. The size of TN2 die is 1200 µm × 600µm.

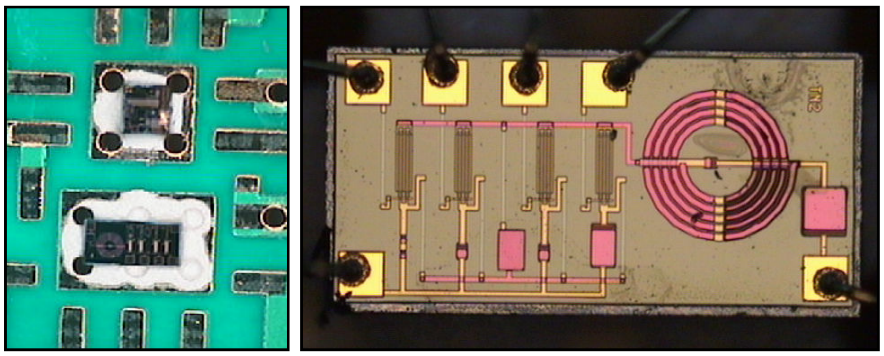


Figure 4.15 Fabricated TN2 die on prototype board

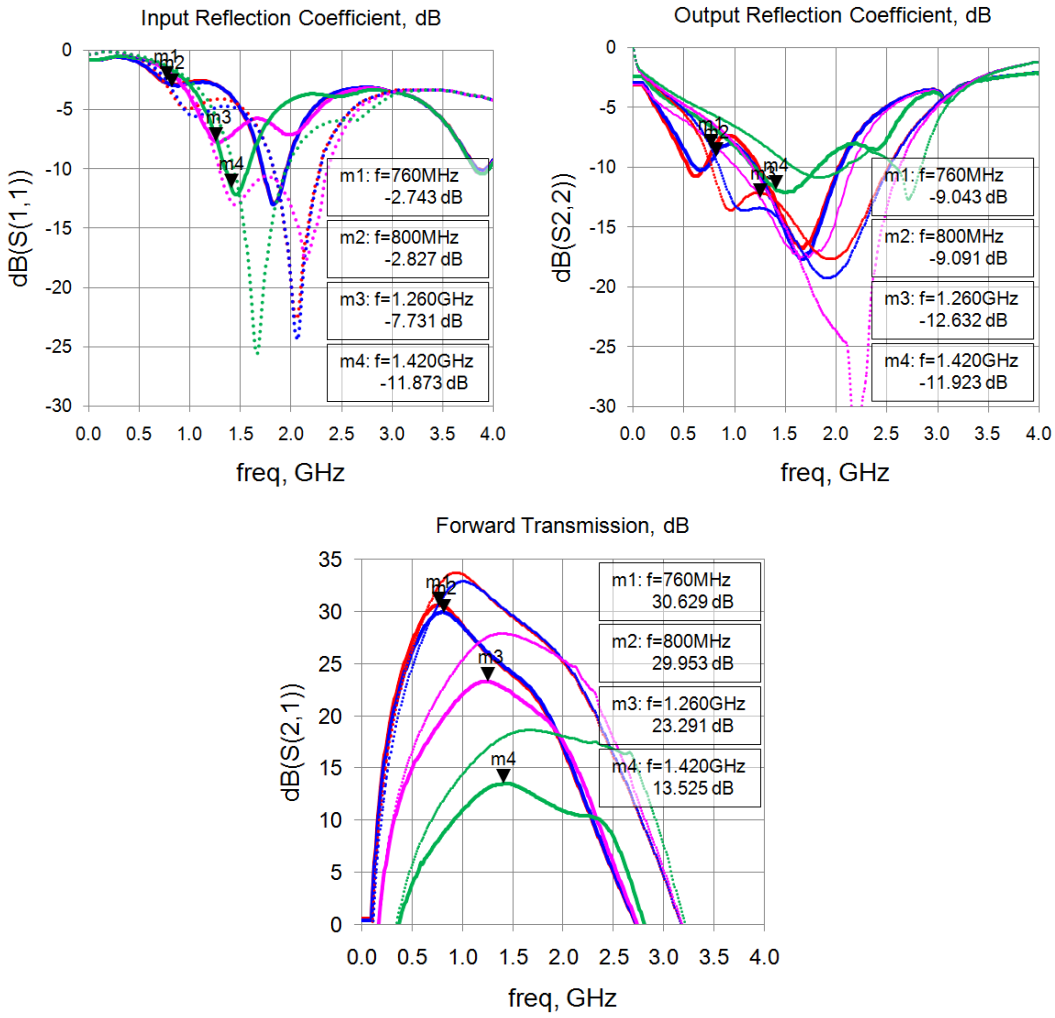


Figure 4.16 Measured Vs. Simulated S-Parameters for TN2

Figure 4.16 shows the measured and simulated S_{21}, S_{11}, and S_{22} at the four center frequencies. In this design, the interstage mismatch loss was not optimized to compensate for the PA gain roll-off which results in gain decrease as increasing

frequency. The fabricated TN2 prototype provides gain that varies from 13 – 30 dB. The input reflection coefficients (S_{11}) vary from -2.7 dB to -11.8 dB. Output reflection coefficients (S_{22}) vary from -9 dB to -11.9 dB. The minimum of reverse isolation (S_{12}) is -41 dB for all states.

The simulated and measured center frequencies and bandwidth are shown in Table 4.15. Table 4.16 shows the simulated gain compression (P_{1dB}) and linearity (OIP3) for TN2. Again, the measured 3-dB bandwidth is less than the simulated 3-dB bandwidth for each center frequency.

Table 4.15 3-dB Bandwidth at varying operating frequencies for TN2

Simulated f_o	940 MHz	1.010 GHz	1.400 GHz	1.670 GHz
Simulated 3-dB BW	680 MHz	760 MHz	1110 MHz	1600 MHz
Measured f_o	760 MHz	800 MHz	1.260 GHz	1.420 GHz
Measured 3-dB BW	580 MHz	630 MHz	910 MHz	1170 MHz

Table 4.16 Measured P_{1dB} and OIP3 of Reconfigurable MMIC PA for TN2

Operating Freq (f_o)	760 MHz	800 MHz	1.260 GHz	1.420 GHz
Simulated P_{1dB} (dBm)	24.123	24.052	24.194	19.409
Measured P_{1dB} (dBm)	24.07	24.15	20.67	15.57
Simulated OIP3 (dBm)	37.631	37.450	36.431	32.131
Measured OIP3 (dBm)	35.89	35.585	35.32	26.785

4.2.2 TN31 with Amp_B

TN31 is a tunable interstage matching network designed to complement the two-stage amplifier Amp_B. This variant uses π-section topology and switched series capacitors to obtain its responses. The total series capacitance value is varied using series FET switches. This variant is realized using MMIC power amplifier and MMIC interstage matching network.

A schematic diagram of the reconfigurable power amplifier using TN31 tunable interstage matching network is shown in Figure 4.17. To operate the amplifier with variant TN31, the following bias voltages are applied: 1) Input bias V_{in} = *5 V* (I_{in} = *15.29 mA*), 2) Output1 bias V_{out1} = *5 V* (I_{out1} = *67.67 mA*), and 3) Output2 bias V_{out2} = *5 V* (I_{out2} = *161.8 mA*). The control voltages applied at the gate terminal of the FET switches are 0 V for on-state and -2 V for off-state. Table 4.17 shows binary combinations of control voltages (V_1, V_2, V_3 and V_4) for TN31 and the corresponding operating frequencies. Other combinations of control voltages result in one of the aforementioned operating frequencies or slightly different.

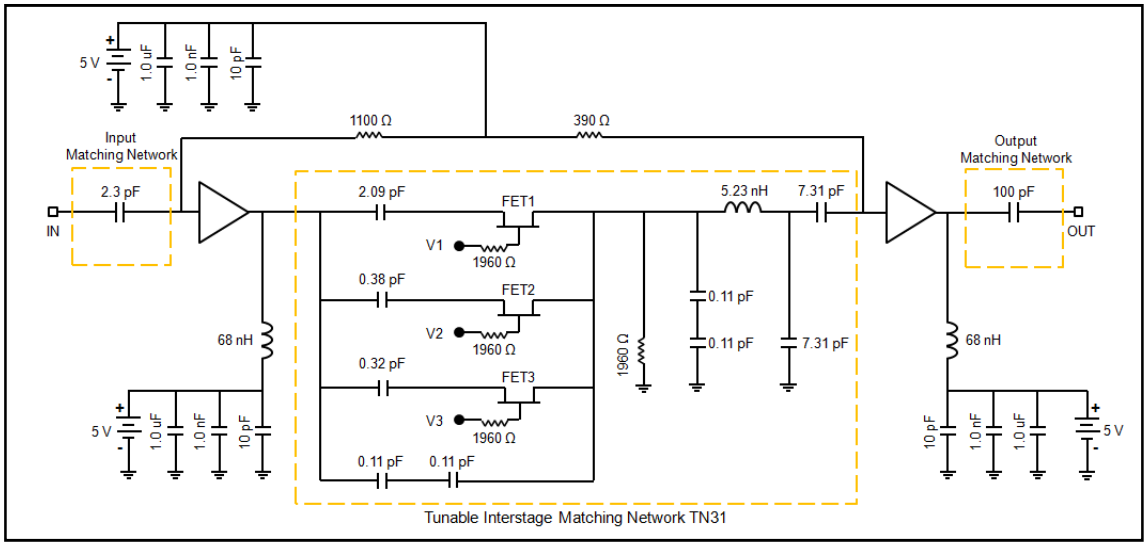


Figure 4.17 Schematic Diagram of Reconfigurable PA with TN31 Interstage Matching Network

Table 4.17 Binary combinations of FET states for TN31

FET 1	FET 2	FET 3	Overall Capacitance	Operating Frequency (f_o)
on	on	on	2.845 pF	720 MHz
on	off	off	2.090 pF	780 MHz
off	on	on	0.755 pF	1.010 GHz
off	off	off	0.055 pF	1.000 GHz

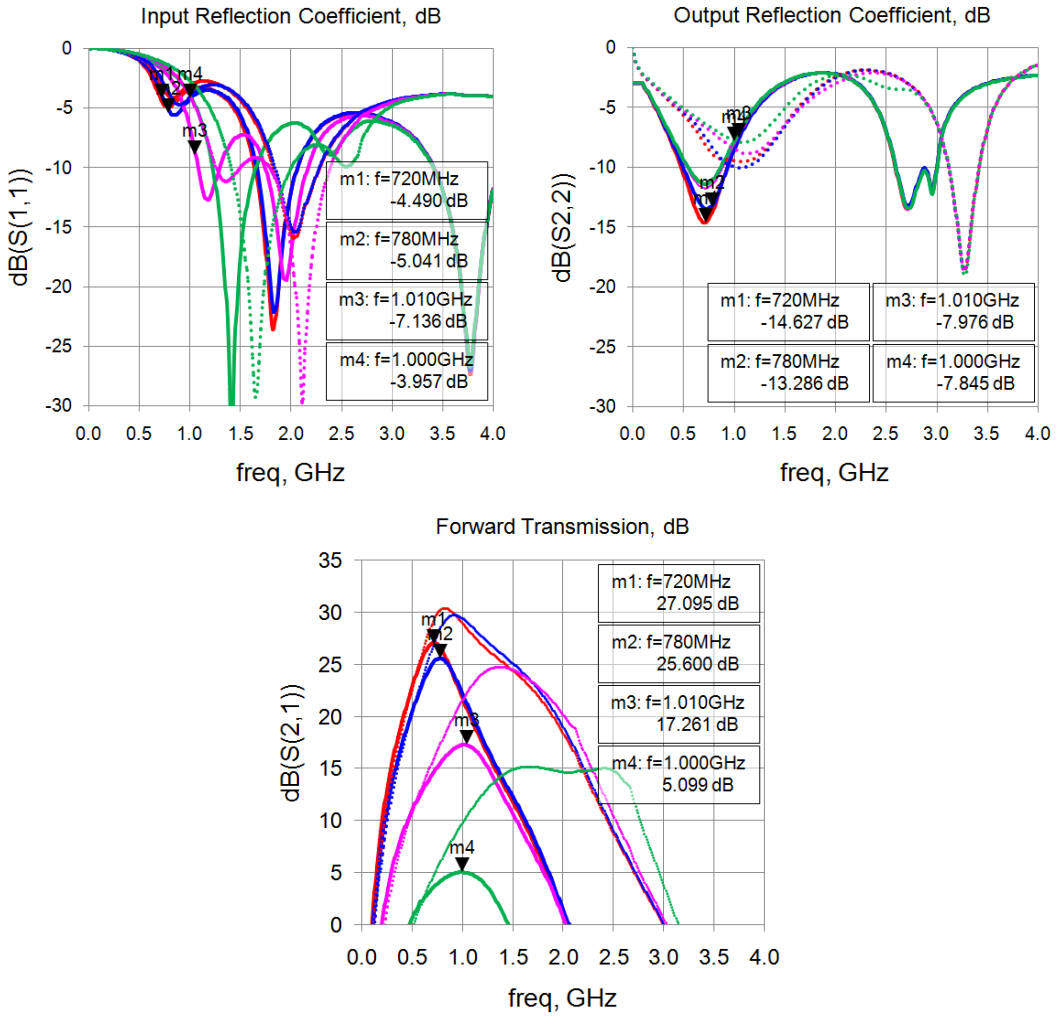


Figure 4.18 Measured Vs. Simulated S-Parameters for TN31

Figure 4.18 shows both measured and simulated S_{21}, S_{11}, and S_{22} at the four center frequencies. In this design, the interstage mismatch loss was not optimized to compensate the PA gain roll-off. The fabricated TN31 prototype provides gain that varies from 5 – 27 dB. The input reflection coefficients (S_{11}) vary from -4 dB to -7.1

dB. Output reflection coefficients (S_{22}) vary from -7.8 dB to -14.6 dB. The minimum of reverse isolation (S_{12}) is -46 dB for all states.

The simulated and measured center frequencies, the corresponding bandwidth and Q-factor are shown in Table 4.18. Table 4.19 shows the simulated gain compression (P_{1dB}) and linearity (OIP3) for TN31.

Table 4.18 3-dB Bandwidth at varying operating frequencies for TN31

Simulated f_o	830 MHz	920 MHz	1.370 GHz	1.660 GHz
Simulated 3-dB BW	510 MHz	610 MHz	860 MHz	1530 MHz
Measured f_o	720 MHz	780 MHz	1.010 GHz	1.000 GHz
Measured 3-dB BW	370 MHz	410 MHz	620 MHz	780 MHz

Table 4.19 Measured P_{1dB} and OIP3 of Reconfigurable MMIC PA for TN31

Operating Freq (f_o)	720 MHz	780 MHz	1.010 GHz	1.000 GHz
Simulated P_{1dB} (dBm)	23.560	23.607	22.706	18.294
Measured P_{1dB} (dBm)	22.80	24.49	24.81	25.29
Simulated OIP3 (dBm)	36.508	36.147	35.180	29.965
Measured OIP3 (dBm)	30.27	32.265	34.385	36.195

Figure 4.19 shows the photo of fabricated TN31 die co-located with the two-stage power amplifier. The size of TN31 die is 1200 µm × 600µm.

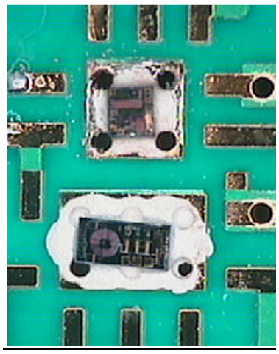


Figure 4.19 Fabricated TN31 die on prototype board

4.2.3 TO0 with Amp_A

TO0 is a tunable interstage matching network designed to complement the two-stage amplifier Amp_A. This variant uses π-section topology and designed for higher frequency band (f_0 > 1 GHz). The total series capacitance value is varied using series FET switches. This variant is realized using MMIC power amplifier and MMIC interstage matching network.

The first step was the initial circuit designs that include the ballasting and biasing network for the two-stage amplifier and wideband matching networks using 3 components forming highpass structure in the input and 3 components forming lowpass structure in the output as elaborated in Section 3.1.1. A comprehensive stability analysis was also performed for each amplifier stage and at each tuning states to ensure unconditional stability.

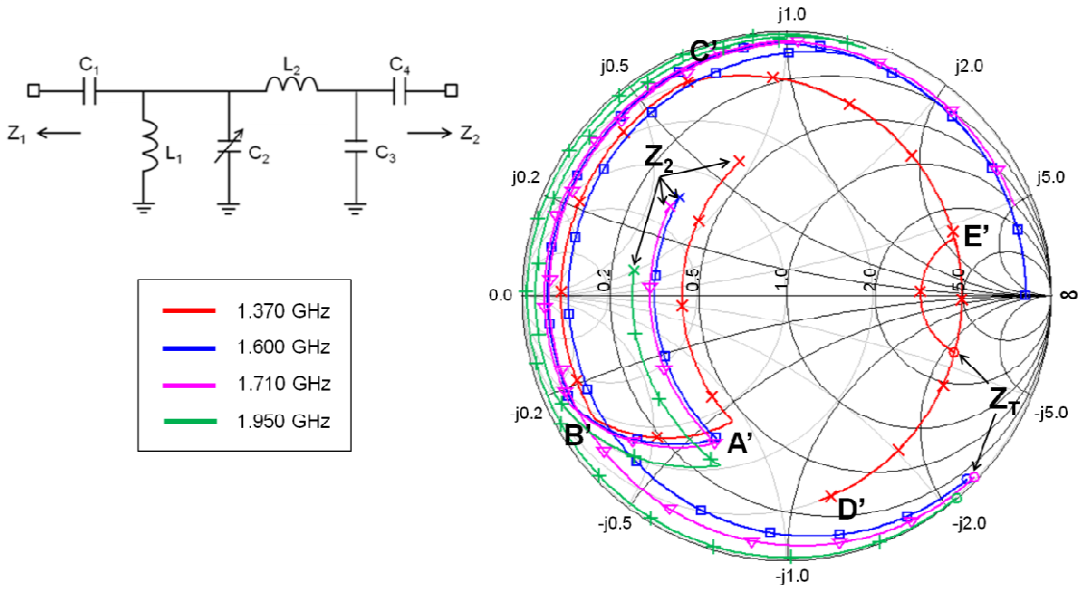


Figure 4.20 π-section impedance transformation at different states for TO0

Figure 4.20 shows the π-section impedance matching network used in the interstage to transform the impedances through lower impedance to reach high Q-contour on the Smith chart. C_4 transforms Z_2 to A', C_3 transforms A' to B', L_2 transforms B' to C', C_2 transforms C' to D', L_1 transforms D' to E', and C_1 transforms E' to Z_T. Besides the transformation purpose, the series capacitors (C_1 and C_4) also behave as DC blocking capacitors. The shunt capacitor C_2 is placed in

parallel with additional 4 shunt capacitors with FET switches in series. Here, the center frequency switching takes place, by varying the capacitance value and thus affecting the mismatch loss at the interstage.

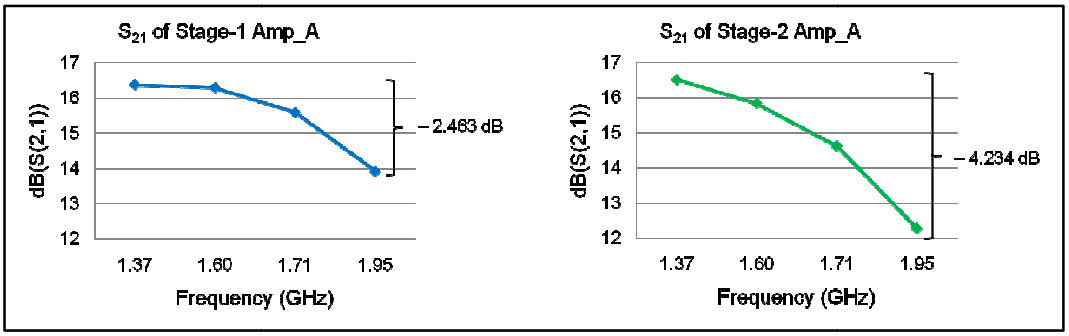


Figure 4.21 Gain Roll-off Analysis for Amp_A

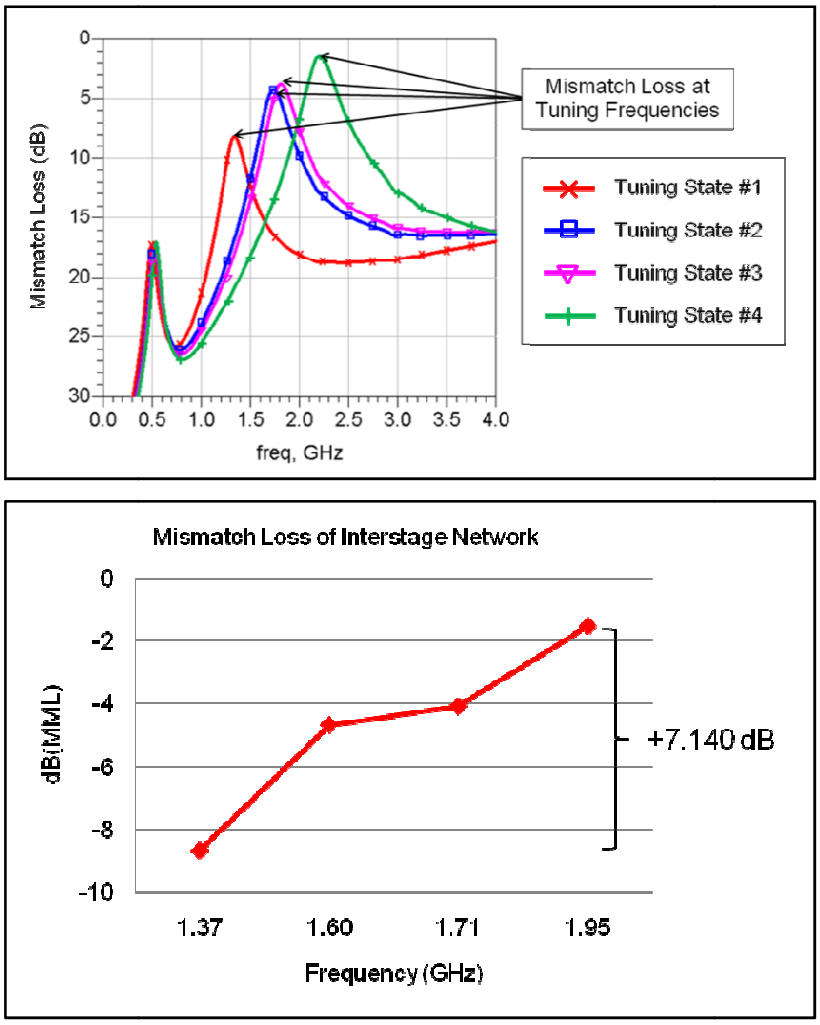


Figure 4.22 Interstage Mismatch Loss for TN0

The gain roll-off at each stage of the amplifier is analyzed by simulating each stage separately. The gain drop between the lowest and highest operating frequency is 2.463 dB in stage-1 and 4.234 dB in stage-2 as shown in Figure 4.21. The total gain drop across the tuning bandwidth is 6.697 dB.

Table 4.20 Interstage Mismatch Loss for TN0

Operating Freq (f_o)	Mismatch Loss
1.37 GHz	8.672 dB
1.60 GHz	4.668 dB
1.71 GHz	4.074 dB
1.95 GHz	1.532 dB

Equation (4.1) is used to computes the mismatch loss between two complex impedances $Z_1 = R_1 + jX_1$ and $Z_2 = R_2 + jX_2$. Total interstage mismatch loss is shown in Table 4.20 and illustrated in Figure 4.22. The circuit was designed for higher mismatch loss at the lower operating frequencies. The mismatch loss at the lowest operating frequency is about 7 dB higher than the mismatch loss at the highest operating frequency. This value compensates for the total gain roll off in the two amplifier stage resulting in gain equalization.

$$M = \frac{4R_1R_2}{|Z_1 + Z_2|^2} \tag{4.1}$$

A schematic diagram of reconfigurable power amplifier using TO0 tunable interstage matching network is shown in Figure 4.23. To operate the amplifier with variant TO0, the following bias voltages are applied: 1) Input bias V_{in} = 1.4 V (I_{in} = 1.341 mA), 2) Output1 bias V_{out1} = 3.6 V (I_{out1} = 143.6 mA), and 3) Output2 bias V_{out2} = 3.6 V (I_{out2} = 268.6 mA). The control voltages applied at the gate terminal of FET switches were 2 V for on-state and -2 V for off-state. Table 4.21 shows binary combinations of control voltages (V_1, V_2, V_3 and V_4) for TO0 and the corresponding operating frequencies. Other combinations of control voltages result in one of the aforementioned operating frequencies or slightly different.

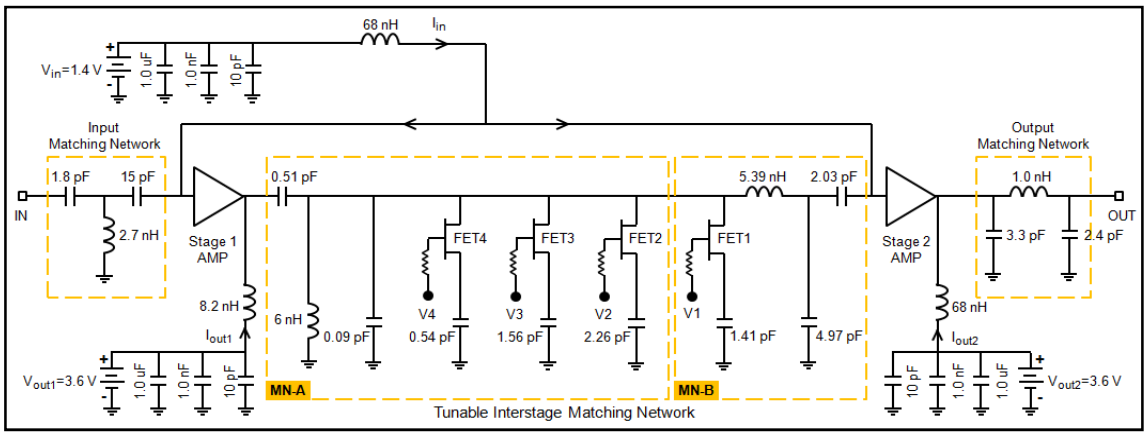


Figure 4.23 Schematic Diagram of Reconfigurable MMIC PA

Table 4.21 Binary combinations of FET states for TO0

FET 1	FET 2	FET 3	FET 4	Overall Shunt Capacitance	Operating Frequency (f_o)
on	on	on	on	5.86 pF	1.37 GHz
on	off	off	on	2.04 pF	1.60 GHz
on	off	off	off	1.50 pF	1.71 GHz
off	off	off	off	0.09 pF	1.95 GHz

The MMIC PA design having 2 gain stages and an interstage matching topology was fabricated and measured. The MMIC PA and MMIC tuner were fabricated using three different die and co-located on the prototype board as shown in Figure 4.24. The die on left side is a 2-stage power amplifier with the dimensions of 720 µm × 660 µm and the two tuner dice on the right side are 600 µm × 600 µm. These two dies form the tunable interstage matching network that provides center frequency tuning function. They were connected using wirebond due to limited resource area. Separate dice for the tuner were necessary because of limited wafer space.

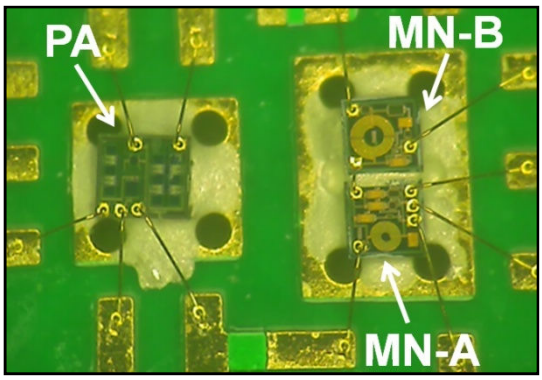


Figure 4.24 Fabricated die TO0 with AMP_A

The Quasi-MMIC design occupies smaller area compared to the previous discrete designs and it gives better corroboration between the measured and simulated responses. For the Quasi-MMIC implementation, the total circuit layout area is about 1.5 mm × 2.5 mm that is 25 times smaller area compared to the discrete implementation. Table 4.22 shows the 3-dB bandwidth at each operating frequency.

Table 4.22 3-dB Bandwidth at varying operating frequencies for TO0

Simulated f_o	1.320 GHz	1.550 GHz	1.700 GHz	2.030 GHz
Simulated 3-dB BW	200 MHz	230 MHz	270 MHz	320 MHz
Measured f_o	1.370 GHz	1.600 GHz	1.710 GHz	1.950 GHz
Measured 3-dB BW	260 MHz	260 MHz	270 MHz	320 MHz

Figure 4.25 show both measured and simulated S_{21}, S_{11}, and S_{22} at the four center frequencies. The solid lines indicate measured data and dotted lines indicate the simulated data. The fabricated prototype provides average of 17 dB ($\pm$ 0.7 dB) gain which gives reasonable agreement with the simulated data. The reconfigurable PA with interstage matching network operates at 1.37 GHz, 1.60 GHz, 1.71 GHz, and 1.95 GHz. The input reflection coefficient (S_{11}) provides less than -10 dB at nearly all operating frequencies. Output reflection coefficient (S_{22}) varies from -8.5 dB to -26.5 dB at different operating frequencies. The minimum of reverse isolation (S_{12}) is -50 dB at all states.

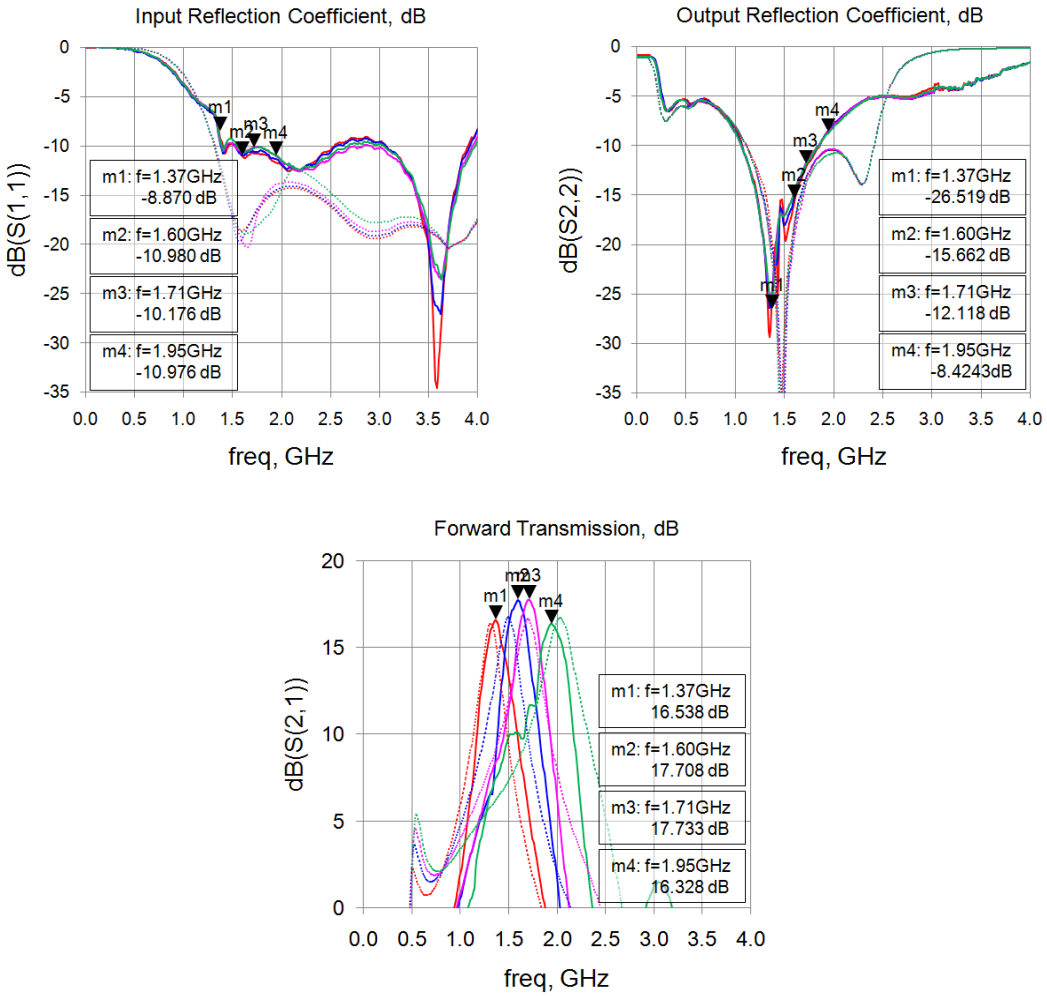


Figure 4.25 Measured vs. Simulated S-parameter of Reconfigurable MMIC PA

Agilent MXA N9020A Spectrum Analyzer and Agilent MXG N5181A Analog Signal Generator were used to measure large signal power handling. OIP3 and P_{1dB} for each state were measured at the corresponding operating frequency (f_o) and the resulting data are tabulated in Table 4.23. The simulated and measured large signal performance gives a good match. Maximum measured OIP3 and P_{1dB} are 28.257 dBm and 16.62 dBm, respectively. Additional losses in the measured circuit (e.g. SMA connectors) account for the slight discrepancy between measured and simulated P_{1dB}.

There is a 2.77 dB variation in the measured P_{1dB} at the lowest and highest operating frequency. This variation could be minimized by tuning the components value in the output matching network. However, the SMT component value that is required for maximum P_{1dB} and minimum P_{1dB} variation is not commercially

available. Figure 4.26 shows the output power for each amplifier stage with input power of 8 dBm at each operating frequency. Stage-1 amplifier shows 1.122 dB decrease and stage-2 amplifier shows 2.053 dB decrease in the output power at the highest operating frequency. The total output power drop at highest operating frequency is 3.175 dB which is consistent with the measured output power variation.

Table 4.23 Measured P_{1dB} and OIP3 of Reconfigurable MMIC PA

Operating Frequency (f_o)	1.370 GHz	1.600 GHz	1.710 GHz	1.950 GHz
Simulated P_{1dB} (dBm)	17.262	17.186	15.282	14.790
Measured P_{1dB} (dBm)	16.62	16.35	14.95	13.85
Simulated OIP3 (dBm)	27.959	24.476	23.024	20.997
Measured OIP3 (dBm)	28.257	25.897	24.832	22.616

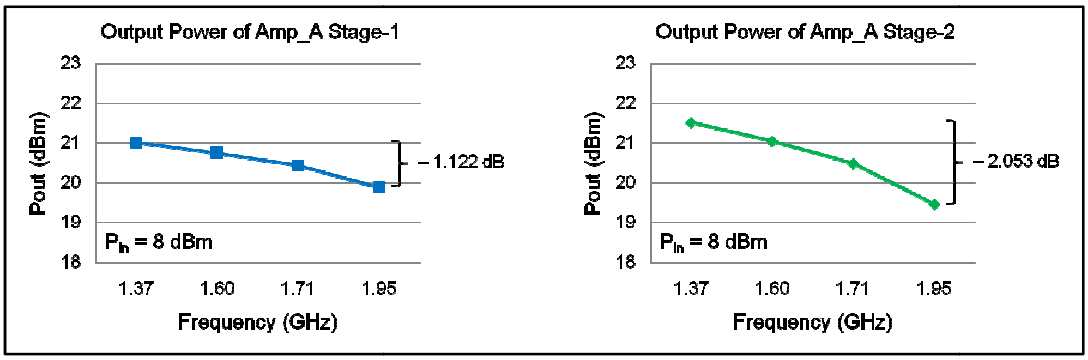


Figure 4.26 Fundamental Output Power of Amp_A

4.3 Effects of Prototype Board Model

The prototype boards were modeled using two methods: 1) CPW model available in ADS and 2) full-wave Electromagnetic simulator in Sonnet™ as discussed in Section 3.6. For discrete designs that operate at lower frequency, the simulation using CPW model and EM-simulated model do not show any significant difference. However, at higher frequency operation, these models show different responses as shown in Figure 4.27.

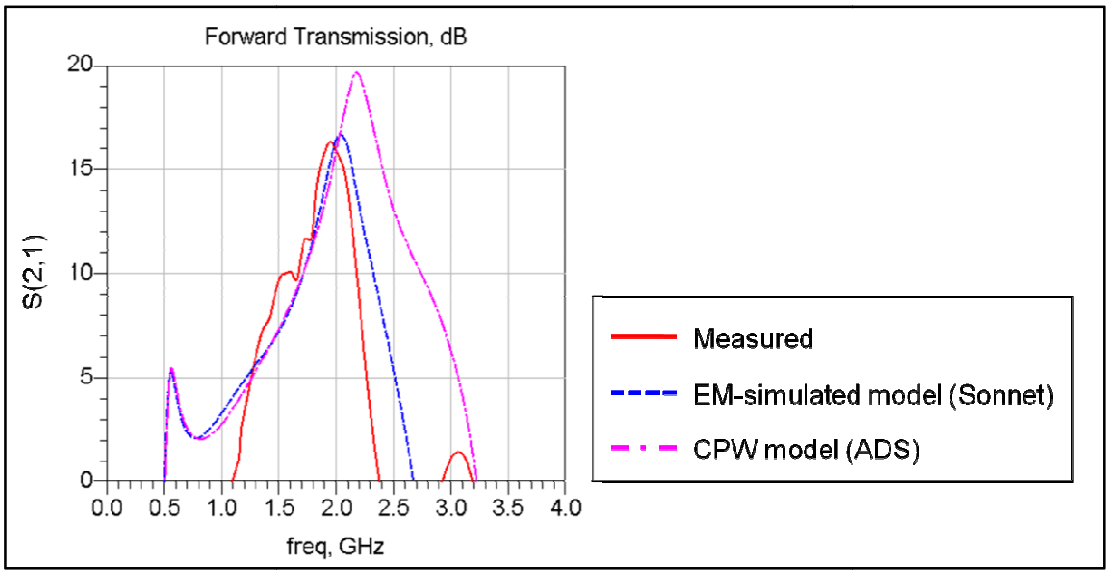


Figure 4.27 CPW Model vs. EM-simulated Model for Prototype Board

As shown in Figure 4.27, the S_{21} response of EM-simulated model is closer to the measured data. The transmission lines on the prototype boards were designed as a grounded CPW structure (grounded metal on the sides of the lines) wherever is possible. For the grounded CPW structure, both microstrip and coplanar waveguide modes are excited. However, at the center of the prototype board, wirebond connections between the metal runner to the bondpads on the MMIC die cause inconsistency to the CPW mode. The improper transmission lines modeling on the prototype board caused the difference in the simulation using CPW-model and EM-simulated model.

This chapter discusses and analyzes the results of the fabricated prototypes. There are 6 prototype variants discussed that include the discrete design (DTN1, DTN2, DTN3), the first MMIC design (TN21, TN3) and the final optimized MMIC design (TO0).

The simulations of the discrete designs give close agreement with the measured response. The discrete designs are suitable for lower operating frequencies because of the size limitation and higher parasitic effects introduced by discrete components. The Quasi-MMIC design is able to operate at higher frequencies (TO0 operates up to 2GHz). The mismatch loss was exploited to compensate PA gain roll-off and reduces the gain fluctuation and equalizes the gain at different operating frequencies with the maximum variation of $\pm$ 0.7 dB. The total layout area of the Quasi-MMIC design is 25 times smaller than the discrete design which gives closer agreement between simulated and measured data compared to the discrete design. Even though the discrete design is easy to fabricate, the Quasi-MMIC design has the advantage of less power consumption because the SP4T switch requires an extra supply voltage of 5 V.

CHAPTER 5

PROPOSED INTEGRATED RECONFIGURABLE GaAs MMIC POWER AMPLIFIER DESIGN

This chapter discusses the conceptual design of an integrated reconfigurable GaAs MMIC power amplifier. The circuit design methodology uses the Smith Chart with mismatch loss exploitation and is discussed in this section. The design layout for the GaAs MMIC die with dimension of 600 μm × 1200 μm is also presented.

5.1 Circuit Design

This section shows the circuit design of Integrated Reconfigurable Power Amplifier. The reconfigurable power amplifier was designed to operate at frequency between 1.0 GHz to 1.7 GHz. The two-stage amplifier and tunable interstage matching network are integrated into a single die while the input and output matching networks are external components.

The first step was the initial circuit designs, the device used for the stage-1 amplifier is 8 fingers FET with unit gate width of 125 μm and the device used for the stage-2 amplifier is 10 finger FET with unit gate width of 100 μm. The design also includes biasing network for the two-stage amplifier is also and wideband matching networks at the input/output side. The input matching network is a 2 stages L-section lowpass structure and a series inductor is placed in the output matching network that match the impedance to 50 Ω. The integrated design uses π-section topology in the interstage. The interstage network uses 3 control FETs (4 × 125 μm) to vary the shunt capacitance value. The components value in the input and output networks were tuned along the process of interstage network design to ensure good return loss. Figure 5.1 shows the integrated schematic design in ADS.

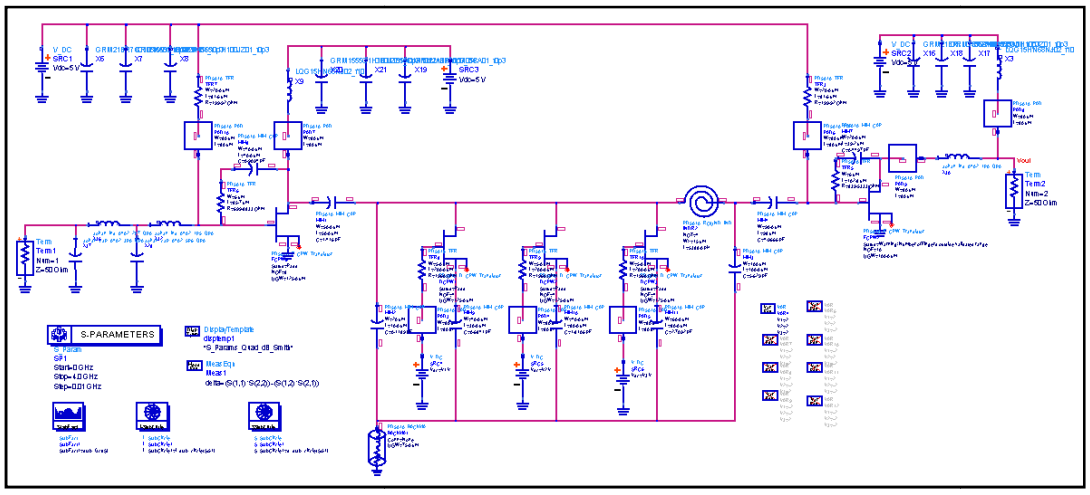


Figure 5.1 Schematic of Interstage Design in ADS

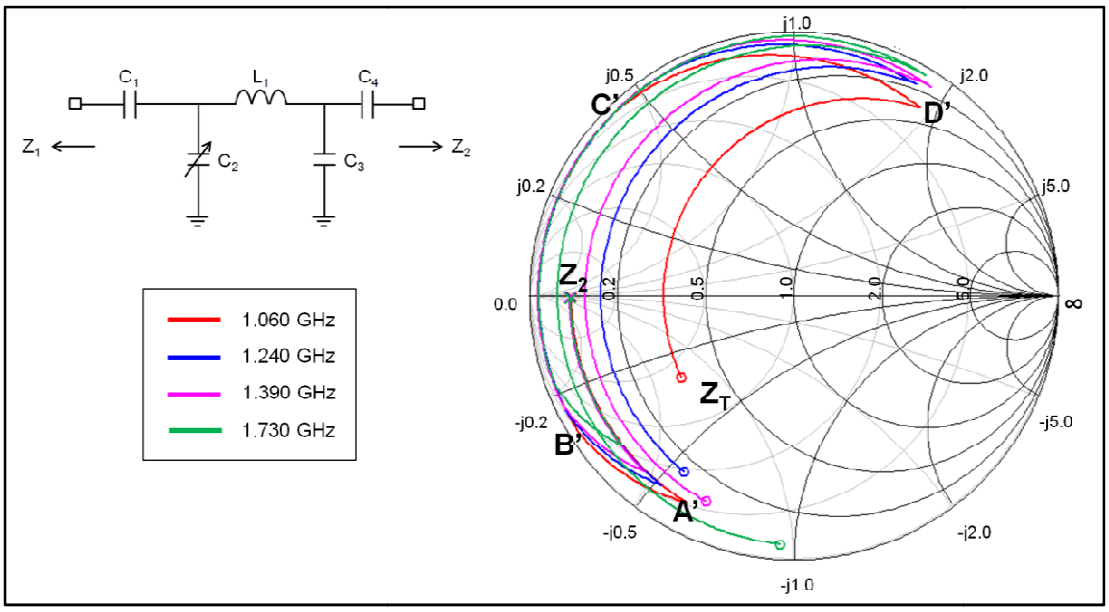


Figure 5.2 π-section Impedances Transformation for Integrated design

Figure 5.2 shows the π-section impedance matching at the interstage that transforms the impedances to reach high Q contour on Smith chart. Series capacitor C_4 transforms Z_2 to *A'*, shunt capacitor C_3 transforms *A'* to *B'*, series inductor L_1 transforms *B'* to *C'*, shunt capacitor C_2 transforms *C'* to *D'*, and series capacitor C_1 transforms *D'* to Z_T. Besides for transformation purposes, series capacitors (C_1 and C_4) also behave as blocking capacitors to avoid the DC path. The shunt capacitor C_2 is placed in parallel with 3 additional shunt capacitors with FET switches in series.

Here, the center frequency switching takes place, by varying the capacitance value and thus affecting the mismatch loss at the interstage.

A complete schematic of the integrated reconfigurable GaAs MMIC power amplifier is shown in Figure 5.3. To operate the amplifier, the following bias voltages are applied: 1) Input bias V_{in} = *5 V* (I_{in} = *39.5 mA)*, 2) Output1 bias V_{out1} = *5 V* (I_{out1} = *238 mA)*, and 3) Output2 bias V_{out2} = *5 V* (I_{out2} = *389 mA)*. The control voltages applied at gate terminal of FET switches were 2 V for the on-state and -2 V for the off-state. Table 5.1 shows binary combinations of control voltages (V_1, V_2 and V_3) used and the corresponding operating frequencies. Other combinations of control voltages result in tuning one of the aforementioned operating frequencies with or without a slight frequency shift.

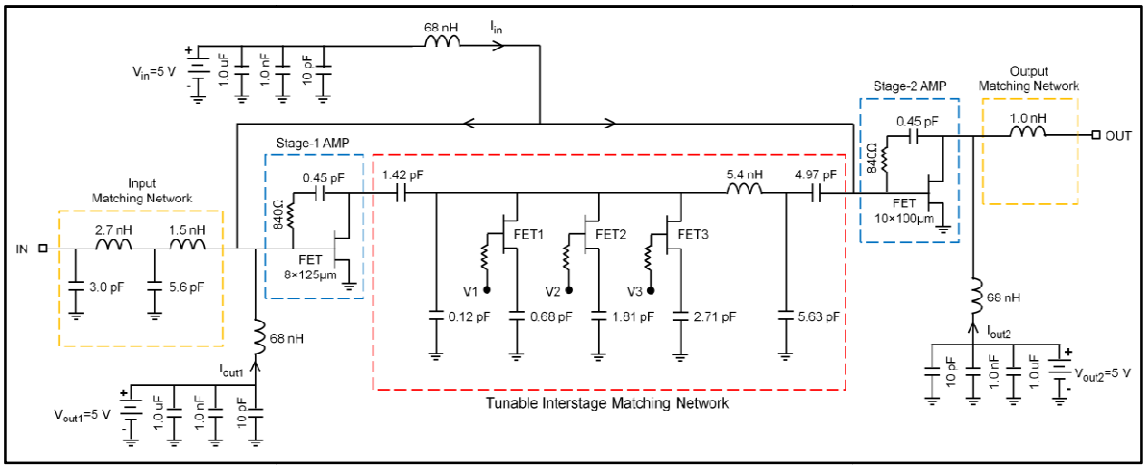


Figure 5.3 Complete Schematic of Integrated Reconfigurable PA

Table 5.1 Binary combinations of FET states

FET 3	FET 2	FET 1	Overall Shunt Capacitance	Operating Frequency (f_o)
on	on	on	5.31	1.060 GHz
on	off	off	2.82	1.240 GHz
off	on	off	1.93	1.390 GHz
off	off	on	0.80	1.730 GHz

The gain roll-off at each stage of the amplifier is analyzed by simulating each stage separately. The impedances in Table 5.2 are used to perform the gain drop analysis as explained in Section 3.1.3. The gain drop between the lowest and highest

operating frequency is 2.045 dB in stage-1 and 2.263 dB in stage-2 as shown in Figure 5.4. The total gain drop across the tuning bandwidth is 4.665 dB.

Table 5.2 Interstage Impedances of Interstage Design

f_0	1.06 GHz	1.24 GHz	1.39 GHz	1.73 GHz
Z_1	9.551 – j1.188	9.254 – j1.422	9.669 + j2.320	13.619 + j4.073
Z_2	33.697 – j5.480	33.726 – j5.785	31.496 – j9.502	27.577 – j9.258
Z_3	102.694 – j81.063	42.478 – j49.038	71.085 – j23.300	48.306 – j11.666
Z_4	35.369 + j0.241	16.657 – j17.713	23.350 – j16.439	15.686 – j20.741
Z_5	4.276 – j0.244	4.265 – j0.245	4.243 – j0.251	4.206 – j0.264
Z_6	50.273 + j6.931	50.289 + j6.755	50.269 + j6.533	50.124 + j6.512

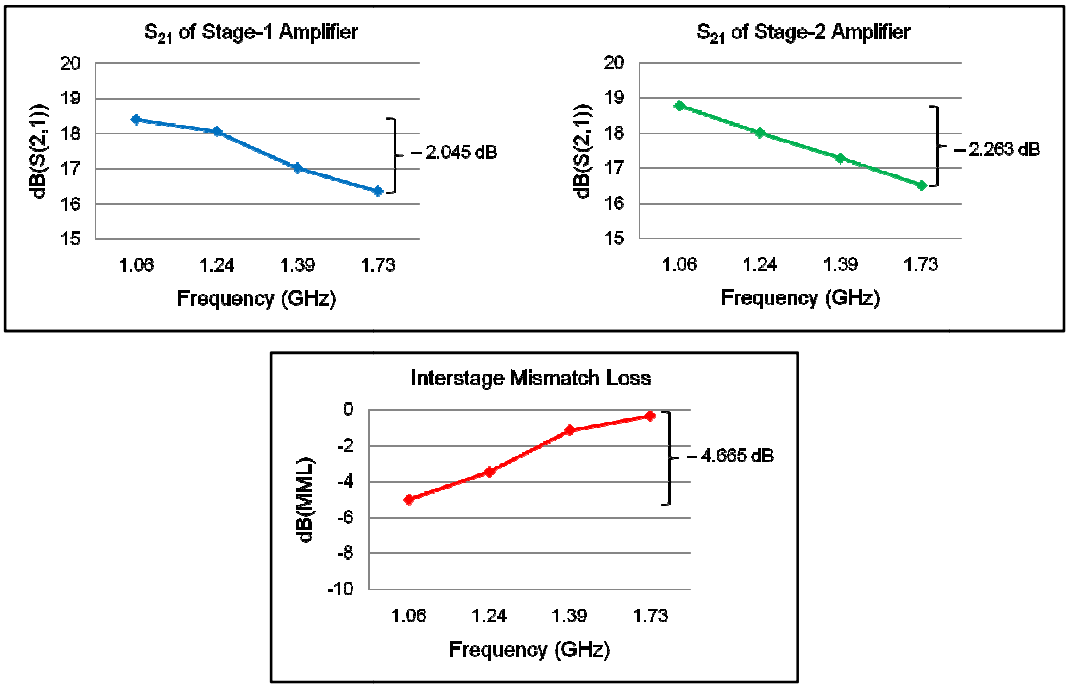


Figure 5.4 Gain Drop Analysis and Interstage Mismatch Loss for Integrated Design

Table 5.3 Interstage Mismatch Loss for Integrated Design

Operating Freq (f_o)	Mismatch Loss
1.06 GHz	5.001 dB
1.24 GHz	3.474 dB
1.39 GHz	1.128 dB
1.73 GHz	0.336 dB

The circuit was designed for higher mismatch loss at the lower operating frequencies to compensate for the gain roll off in the two amplifier stage as shown in Table 5.2.

The average gain at all operating frequencies are therefore equalized to be 21.5 dB (± 0.4 dB) across 48 % tuning bandwidth as shown in Figure 5.5. The integrated reconfigurable PA operates at 1.06 GHz, 1.24 GHz, 1.39 GHz, and 1.73 GHz. The simulated input reflection coefficient (S_{11}) and output reflection coefficient (S_{22}) provides less than -10 dB at all operating frequencies. The minimum of reverse isolation (S_{12}) is -80 dB at all states.

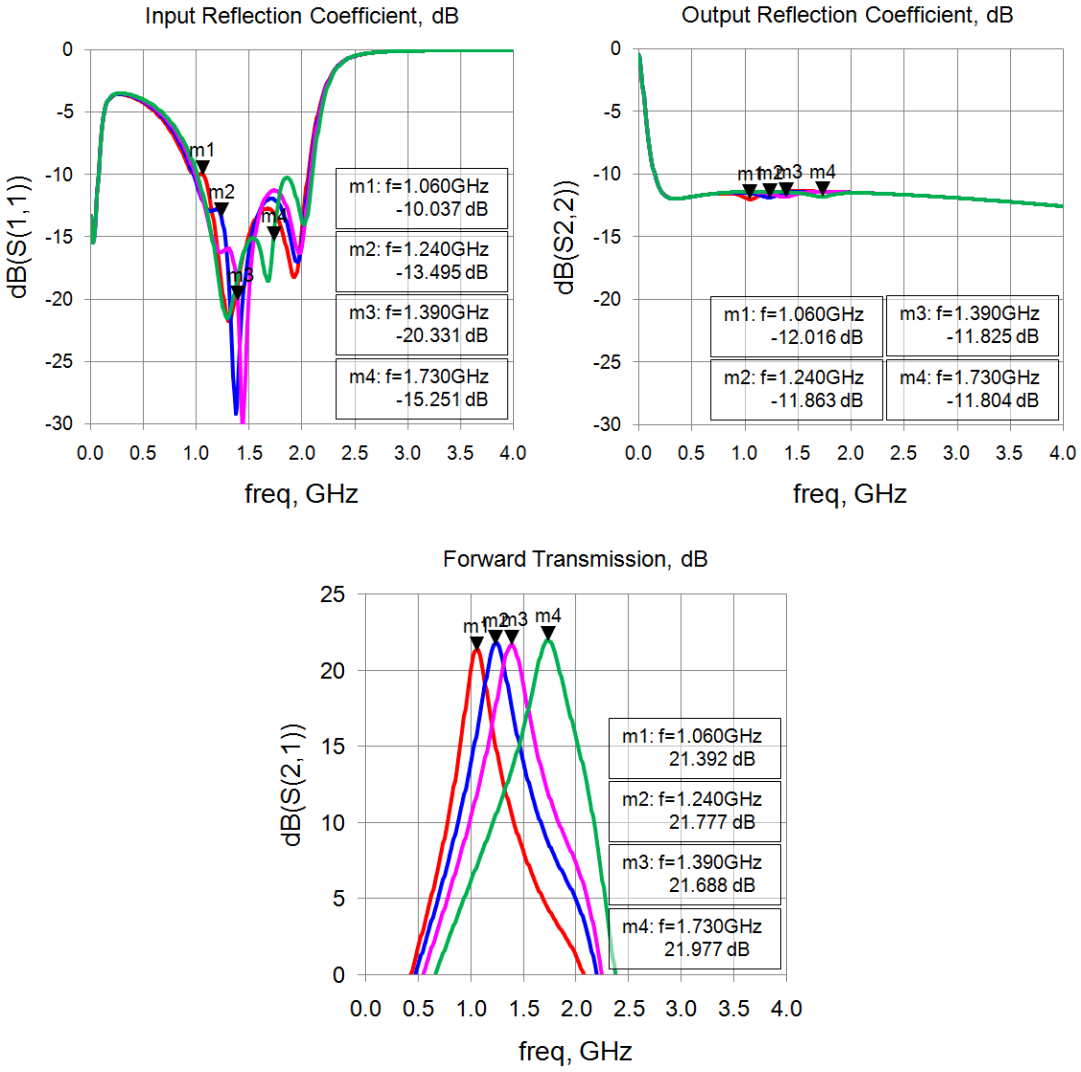


Figure 5.5 Measured vs. Simulated S-parameter of Integrated Reconfigurable PA

The simulated center frequencies, corresponding bandwidth, and Q-factor are shown in Table 5.4. Table 5.5 shows the simulated gain compression (P_{1dB}) and linearity (OIP3) for the integrated reconfigurable PA design.

Table 5.4 3-dB Bandwidth at varying operating frequencies

Simulated f_o	1.060 GHz	1.240 GHz	1.390 GHz	1.730 GHz
Simulated 3-dB BW	200 MHz	240 MHz	260 MHz	290 MHz

Table 5.5 Measured P_{1dB} and OIP3 of Reconfigurable MMIC PA

Operating Frequency (f_o)	1.060 GHz	1.240 GHz	1.390 GHz	1.730 GHz
Simulated P_{1dB} (dBm)	24.944	25.019	25.565	23.323
Simulated OIP3 (dBm)	31.312	31.619	32.686	33.576

5.2 Stability Analysis

A comprehensive stability analysis was also performed for each amplifier stage and at each tuning states to ensure unconditional stability. The K-Δ analysis was performed for 4 configurations (Figure 5.6):

1. First stage amplifier with interstage matching network.
2. Second stage amplifier.
3. Second stage amplifier with interstage matching network.
4. First stage amplifier.

In each configuration, the *K*-Δ analysis was performed for 4 operating states which are indicated in the figures with different colors. For unconditional stability, the value of *K* must be greater than 1 and the magnitude of |Δ| must be less than 1 at all frequencies.

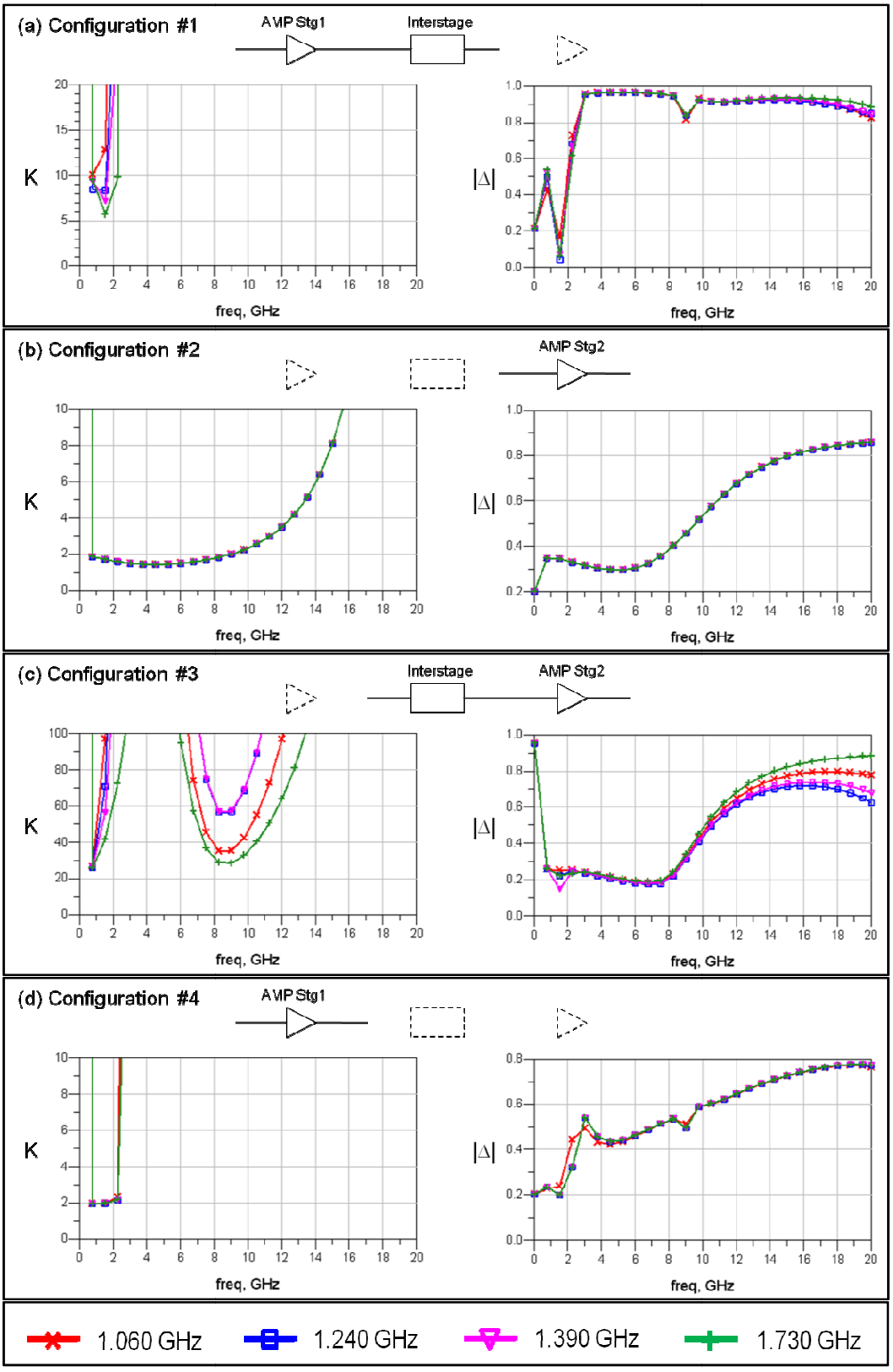


Figure 5.6 K-Δ Stability Analysis for Integrated Reconfigurable PA

5.3 Layout Design

The proposed integrated reconfigurable PA design incorporates the tunable interstage matching network and the two-stage power amplifier onto a single MMIC die. The integrated MMIC die is much smaller than the circuits discussed in Chapter 4. Figure 5.7 shows the layout of the proposed Integrated Reconfigurable PA with dimension of 1200 µm × 600 µm which is 130 times smaller area compared to the discrete design. The area with the red dash-dotted line in Figure 5.7 indicates the location of tunable interstage matching network. The areas with blue dotted lines indicate the first and second stage amplifiers.

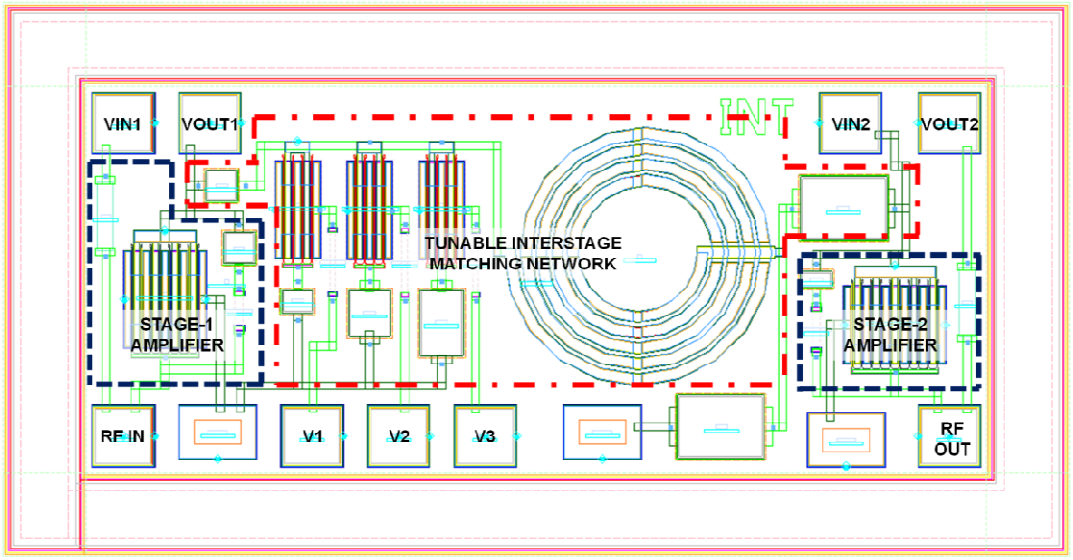


Figure 5.7 Layout Design for Integrated Reconfigurable PA

The proposed integrated design was simulated without the presence of the prototype board. Measurement of the proposed design must be performed using a probe station. It should be noted, however that a test board could be used subsequent to MMIC fabrication to perform additional tuning. Measurement setup using test board for the proposed design is shown in Figure 5.8.

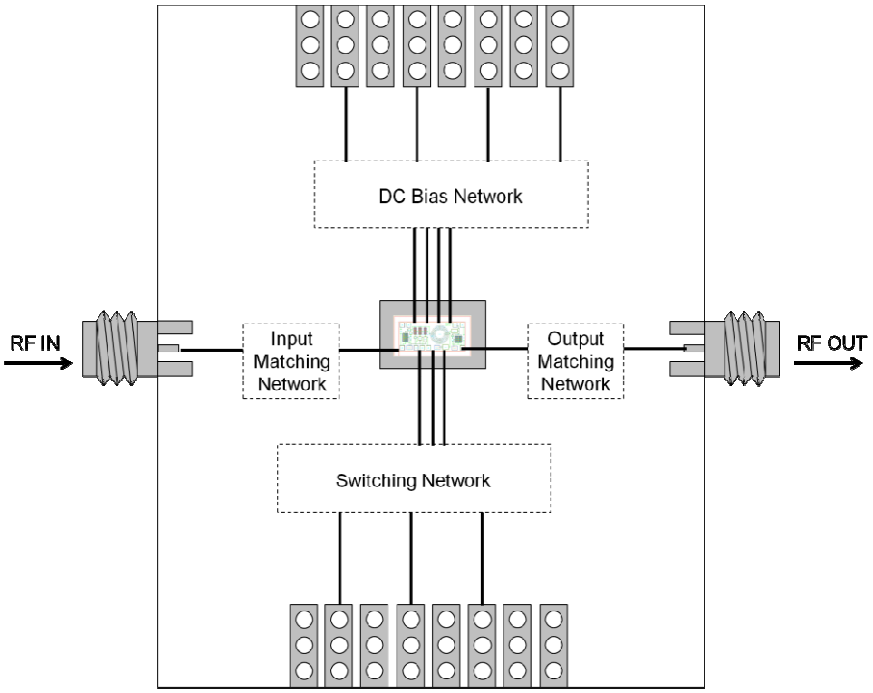


Figure 5.8 Measurement Setup for Integrated Reconfigurable PA using Test Board

This chapter discusses the conceptual design for integrated reconfigurable power amplifier. It includes the initial circuit design of the two-stage amplifier, the graphical method using Smith chart and the gain roll-off calculation for mismatch loss analysis for gain equalization. The amplifier operates from 1.06 GHz to 1.73 GHz (48 % tuning bandwidth) with average gain of 21.5 dB and maximum gain variation between tuning states of $\pm$ 0.4 dB. The large signal data is also simulated and the maximum P_{1dB} and OIP3 are 24.9 dBm and 33.5 dBm. The stability analysis using Rollet's condition is performed to ensure unconditional stability. Finally, the layout for integrated reconfigurable amplifier is designed and the measurement setup is also provided. The total layout area of this design is 1.2 mm × 0.6 mm which is 130 times smaller area compared to the discrete design.

CHAPTER 6

CONCLUSIONS AND RECOMMENDATIONS

This chapter discusses the conclusions and recommendations. The conclusion reviews the objectives of this project followed by a brief discussion on methodology and the result and discussion. The recommendation provides some suggestions on possible future work related to this topic.

6.1 Conclusion

The focus of this work is to exploit the interstage matching network for tuning to build a reconfigurable power amplifier. Two-stage power amplifiers were used in the design. The input and output matching network were fixed while the impedances of interstage matching network were varied using electronic switching.

As mentioned in earlier works [6], [9], [14] – [16], [19], the main problems in reconfigurable devices are the gain fluctuation and bandwidth variation between the tuning states. The circuit design methodology used in this work includes utilization of Smith chart to design interstage matching networks with bandpass structure that reach high Q-contour on the Smith chart. To compensate for gain roll-off from the two-stage amplifier, the mismatch loss in the interstage was controlled to decrease with increasing frequency. M-probe technique was used to calculate the mismatch loss at the interstage without invasion of the circuit performance [75].

The circuit simulation was done using Agilent's Advanced Design System (ADS). Parasitic effects of prototype board were modeled in Sonnet^{TM} EM-solver and the S-parameter block generated was included in the ADS simulation. Sensitivity analysis of long and thin transmission lines was also performed using ADS to ensure negligible effect on the circuit performance.

In this thesis, two different circuit configurations were considered. This includes the design, fabrication and measurement of a discrete design and a partial monolithic design (Quasi-MMIC design). The simulated and measured responses of these designs are documented in Chapter 4.

As a proof of concept, a reconfigurable power amplifier with tunable interstage matching network was first realized by using two-stage MMIC power amplifier and surface-mount (discrete) components for the interstage matching network. Two topologies, T-section and π-section, were used in the interstage. The π-section topology is able to obtain narrower bandwidth compared to T-section topology. The reconfigurable PA using discrete tuner was designed for use at frequencies below 1 GHz where the cognitive radio and power line communication application operate. The advantages of the discrete design are low cost and use of commercially off-the-shelf components (COTS) including the SP4T switch. The total layout area of this discrete design is 7.5 mm × 12.5 mm and there is about 2 dB discrepancy between measured vs. simulated data.

At higher frequencies, the size of discrete components becomes relatively large compared to the wavelength and the surface-mount components can self-resonate. The electromagnetic coupling and parasitic effect from the prototype board become more evident which cause difficulties in design process. Therefore, quasi-MMIC reconfigurable PA was designed for operation at higher frequency to cover GSM900, GSM1800 and WiMAX frequency (0.9 – 2.4 GHz) with $\pm$ 0.7 dB gain variation. The total layout area of the Quasi-MMIC design is 1.5 mm × 2.5 mm (25x smaller area than discrete design) and there is only about 0.65 dB discrepancy between measured vs. simulated data.

Finally, a conceptual design of a fully monolithic reconfigurable PA (Integrated-MMIC design) was discussed in Chapter 5. The circuit layout occupies a single GaAs MMIC die with the dimensions of 600 μm × 1200 μm (130x smaller area than discrete design). By exploiting the mismatch loss, gain equalization is used to reduce the gain variation to only $\pm$ 0.4 dB.

The concept of a reconfigurable power amplifier using tunable interstage matching network has been designed and fabricated. Two configurations using different design methodologies were measured. The discrete design only covers the operation on lower frequency range (f_o < 1 GHz) while the Quasi-MMIC design can cover operating frequencies above 1 GHz. The Quasi-MMIC design offers utilization of FET switches which are fabricated monolithically to control the tuning elements in a reconfigurable power amplifier which simplifies production process and lower the cost. This approach is helped with the design structure that absorbs the FET parasitics into the tuning elements. The Quasi-MMIC design also consumes less power because the switching network of discrete design requires extra supply voltage for the SP4T. The experiments show that as the structure of the reconfigurable power amplifier shrinks, the discrepancy between measured and simulated data also decreases. The smaller structure has less parasitic effect to the reconfigurable power amplifier and enables it to operate at higher frequency.

6.2 Recommendations for Future Work

The following are potential areas to be considered related to utilization of interstage matching network as tuning elements in reconfigurable microwave devices.

6.2.1 Realization of Integrated Reconfigurable Power Amplifier

Due to time and resource limitation, the conceptual design on Integrated Reconfigurable PA using Interstage Matching Network (fully-MMIC design) could not be realized as a fabricated prototype. The design was intended to be measured using probe station as the parasitic effect of prototype board was not included in the design process.

6.2.2 Utilization of Multi-stage Power Amplifier

In this work, only two-stage amplifiers using a single tunable interstage matching network were used in the design. The performance of multi-stage (N>2) amplifiers including interstage matching network should be explored further.

6.2.3 Effects of Input/Output Matching to the Device Reconfigurability

In this work, the interstage is the only matching network with variable impedances while the input and output matching networks are fixed. The effect of wideband matching and narrowband matching network to the device reconfigurability should be further investigated.

APPENDIX A

SKYWORKS SP4T (AS204-80) DATASHEET

DATA SHEET

AS204-80, AS204-80LF: GaAs IC SP4T Nonreflective Switch With Driver 300 kHz–3.5 GHz

Features

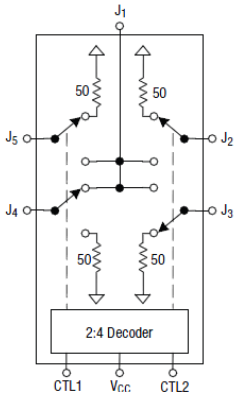
- Integrated driver 5 V supply voltage
- High isolation (45 dB @ 0.9 GHz)
- Low insertion loss (0.5 dB @ 0.9 GHz)
- SSOP-16 plastic package
- Nonreflective all ports
- ESD rated at class 1A HBM
- Available lead (Pb)-free and RoHS-compliant MSL-1 @ 260 °C per JEDEC J-STD-020

Description

The AS204-80 is a high-isolation SP4T FET IC nonreflective switch with driver. The insertion loss is 0.5 dB and isolation is 45 dB at 0.9 GHz. The switch is ideal for cellular base station switch matrices.

NEW Skyworks offers lead (Pb)-free, RoHS (Restriction of Hazardous Substances)-compliant packaging.

Simplified Block Diagram



Electrical Specifications at 25 °C

V_{CC} = 5 V, Z_O = 50 Ω, unless otherwise noted

Parameter[1]	Frequency	Min.	Typ.	Max.	Unit
Insertion loss[2]	300 kHz–1.0 GHz		0.4	0.6	dB
	300 kHz–2.0 GHz		0.6	0.8	dB
	300 kHz–2.5 GHz		0.7	0.9	dB
	300 kHz–3.5 GHz		0.9	1.2	dB
Isolation	300 kHz–1.0 GHz	40	45		dB
	300 kHz–2.0 GHz	30	38		dB
	300 kHz–2.5 GHz	28	32		dB
	300 kHz–3.5 GHz	22	25		dB
VSWR[3] on state	300 kHz–3.5 GHz		1.3:1		
VSWR[3] off state	0.5 GHz–3.5 GHz		1.5:1		

1. All measurements made in a 50 Ω system, unless otherwise specified.
2. Insertion loss changes by 0.003 dB/°C.
3. Input/Output.

Operating Characteristics at 25 °C

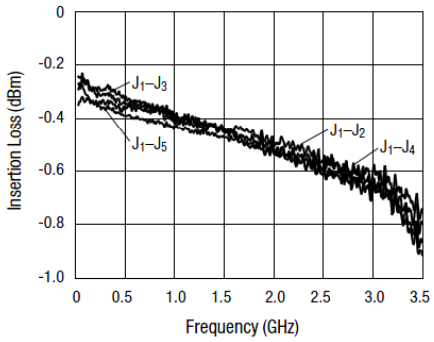
V_{CC} = 5 V, Z_0 = 50 Ω, unless otherwise noted

Parameter	Condition	Frequency	Min.	Typ.	Max.	Unit
Switching characteristics						
Rise, fall	10/90% or 90/10% RF			75		ns
On, off	50% CTL to 90/10% RF			125		ns
Video feedthru	T_{RISE} = 1 ns, BW = 500 MHz			50		mV
Input power for 1 dB compression		0.5–2 GHz		26		dBm
Intermodulation intercept point (IP3)	For two-tone input power 13 dBm	0.5–2 GHz		40		dBm
		0.05 GHz		29		dBm
Thermal resistance				30		°C/W
Control voltages[1]	CTL1, 2 low		0		0.5	V
	CTL1, 2 high		2.4		5.0	V
Supply voltage, V_{CC}[1]			4.8		5.2	
Supply current	V_{CC} = 5 V			500		µA

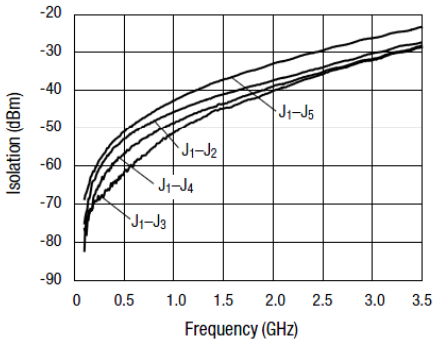
1. V_{CC} must be powered on by a minimum of 10 ns prior to V_{CTL}.

Typical Performance Data

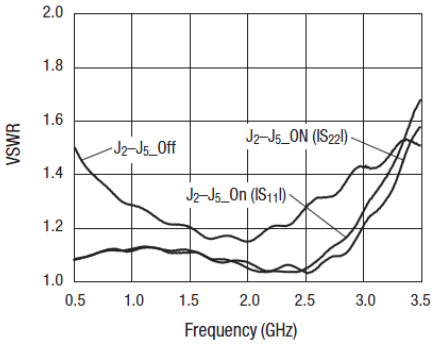
V_{CC} = 5 V, Z_0 = 50 Ω, unless otherwise noted



Insertion Loss vs. Frequency

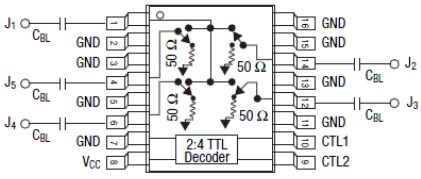


Isolation vs. Frequency



VSWR vs. Frequency

Pin Out



DC blocking capacitors (C_{BL}) required for positive voltage operation.
C_{BL} = 47 pF for operation frequency >500 MHz.

Absolute Maximum Ratings

Characteristic	Value
RF input power	0.8 W > 500 MHz 0.2 W @ 50 MHz
Supply voltage	6 V
Control voltage	-0.2 V, +6 V
Operating temperature	-40 °C to +85 °C
Storage temperature	-65 °C to +150 °C
ESD human body model	Class 1A

Performance is guaranteed only under the conditions listed in the specifications table and is not guaranteed under the full range(s) described by the Absolute Maximum specifications. Exceeding any of the absolute maximum/minimum specifications may result in permanent damage to the device and will void the warranty.

CAUTION: *Although this device is designed to be as robust as possible, ESD (Electrostatic Discharge) can damage this device. This device must be protected at all times from ESD. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions must be employed at all times.*

Recommended Solder Reflow Profiles

Refer to the *"Recommended Solder Reflow Profile"* Application Note.

Tape and Reel Information

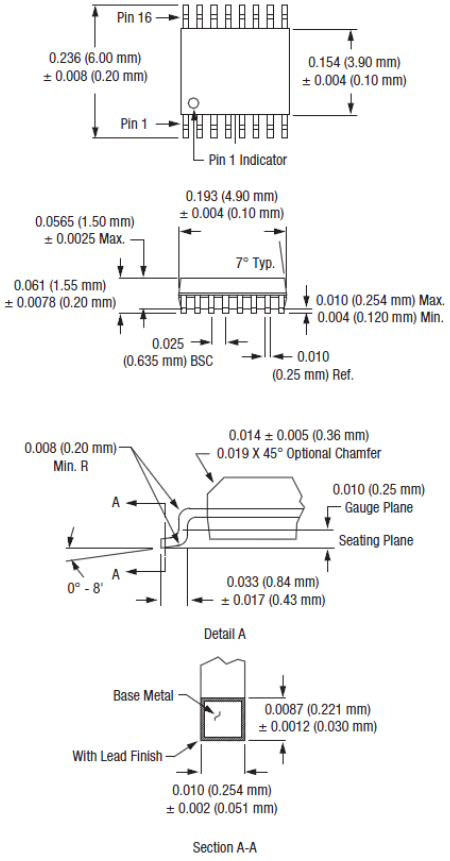
Refer to the *"Discrete Devices and IC Switch/Attenuators Tape and Reel Package Orientation"* Application Note.

Truth Table

Insertion Loss Path J_1 to:	Control Input	
	CTL1	CTL2
J_2	0	0
J_3	1	0
J_4	0	1
J_5	1	1

"0" = 0 to 0.5 V.
"1" = 2.4 to 5 V.

SSOP-16 (-80)



APPENDIX B

TN_PROTOTYPE BOARD LAYOUT

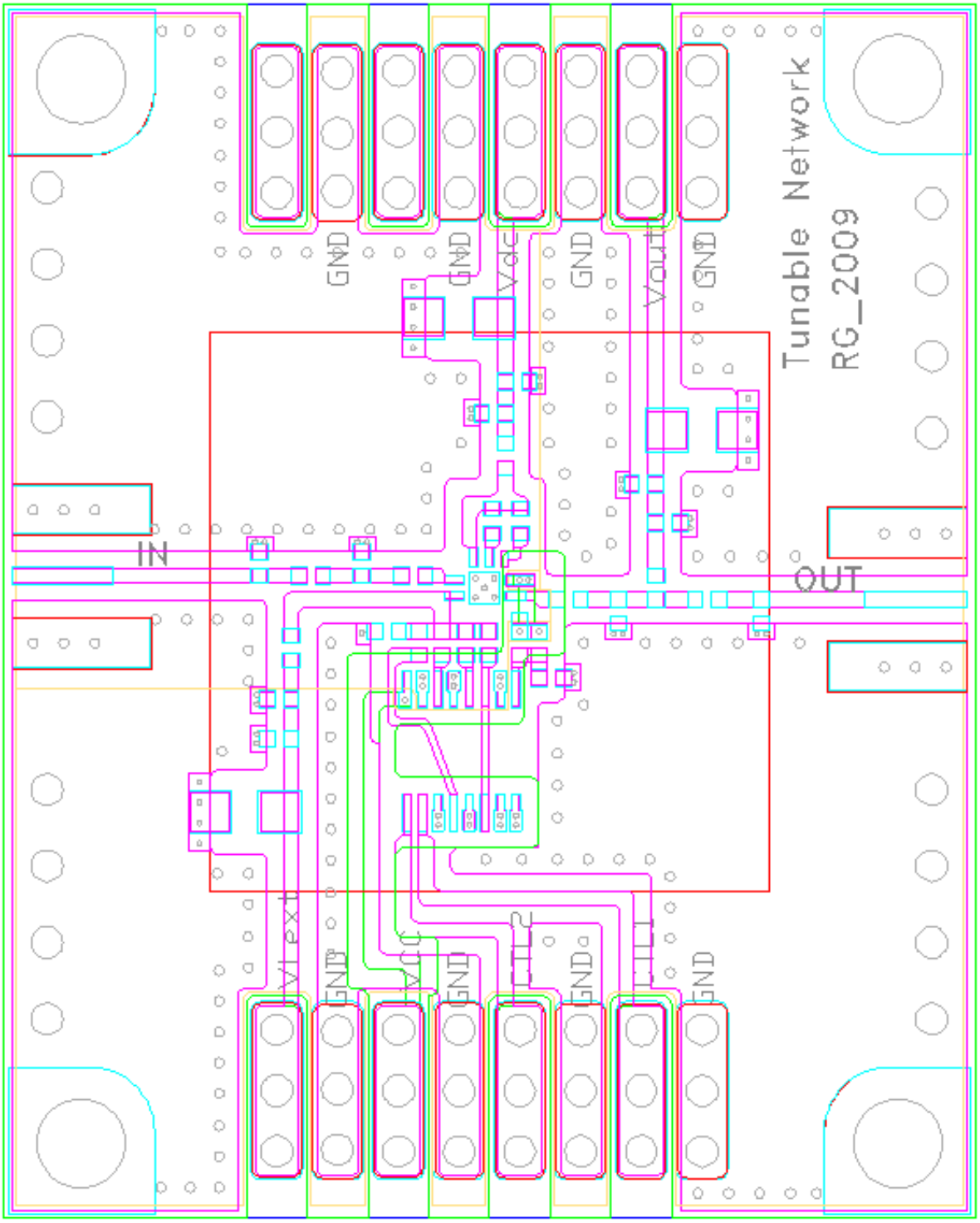


Figure B.1 TN_Prototype1 Board Layout

This board layout was designed to accommodate components of the discrete designs (DTN1, DTN2, and DTN3).

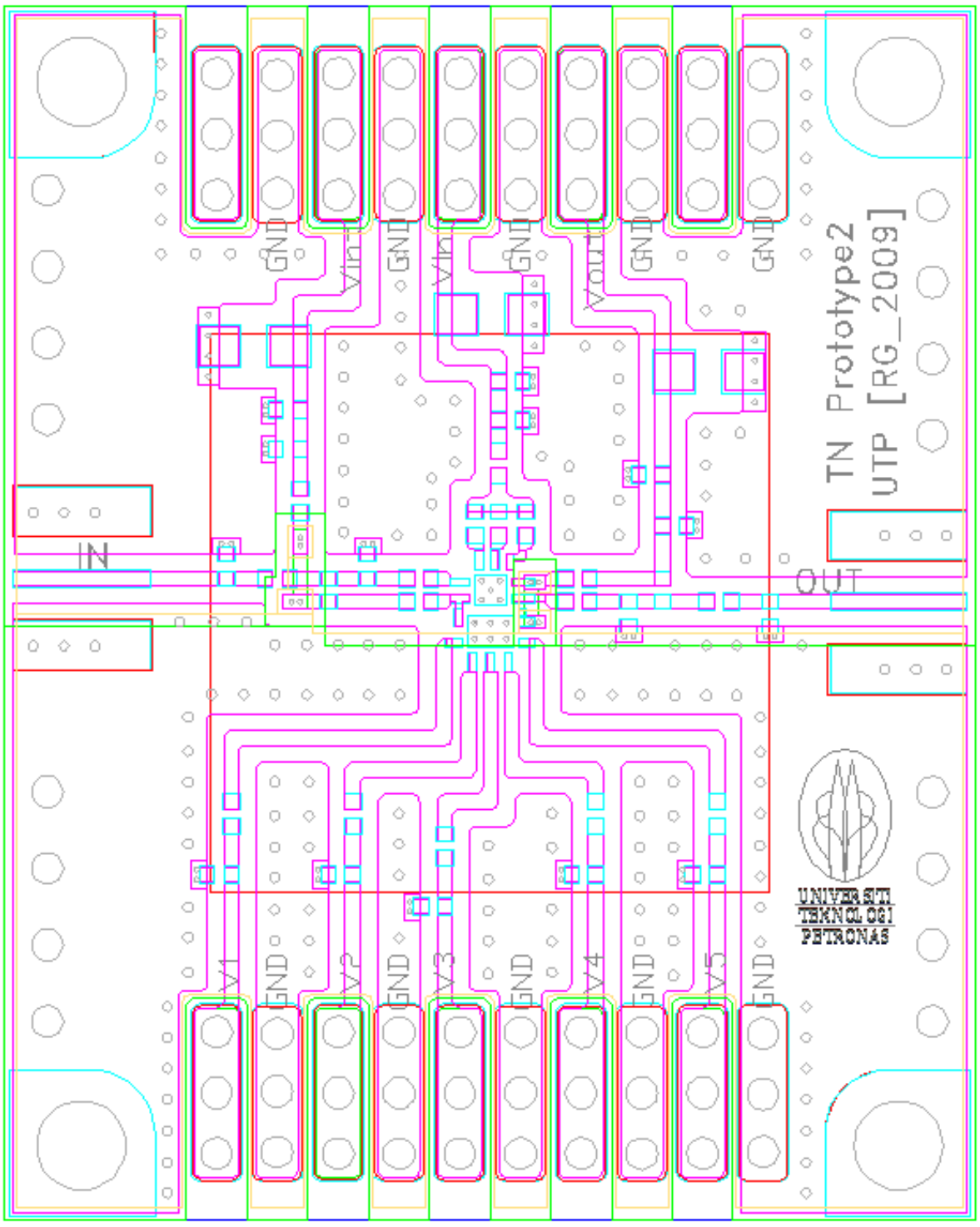


Figure B.2 TN_Prototype2 Board Layout

This board layout was designed to accommodate components of the quasi-MMIC designs (TN2, TN31, and TO0).

APPENDIX C

TN_PROTOTYPE FABRICATION MASK

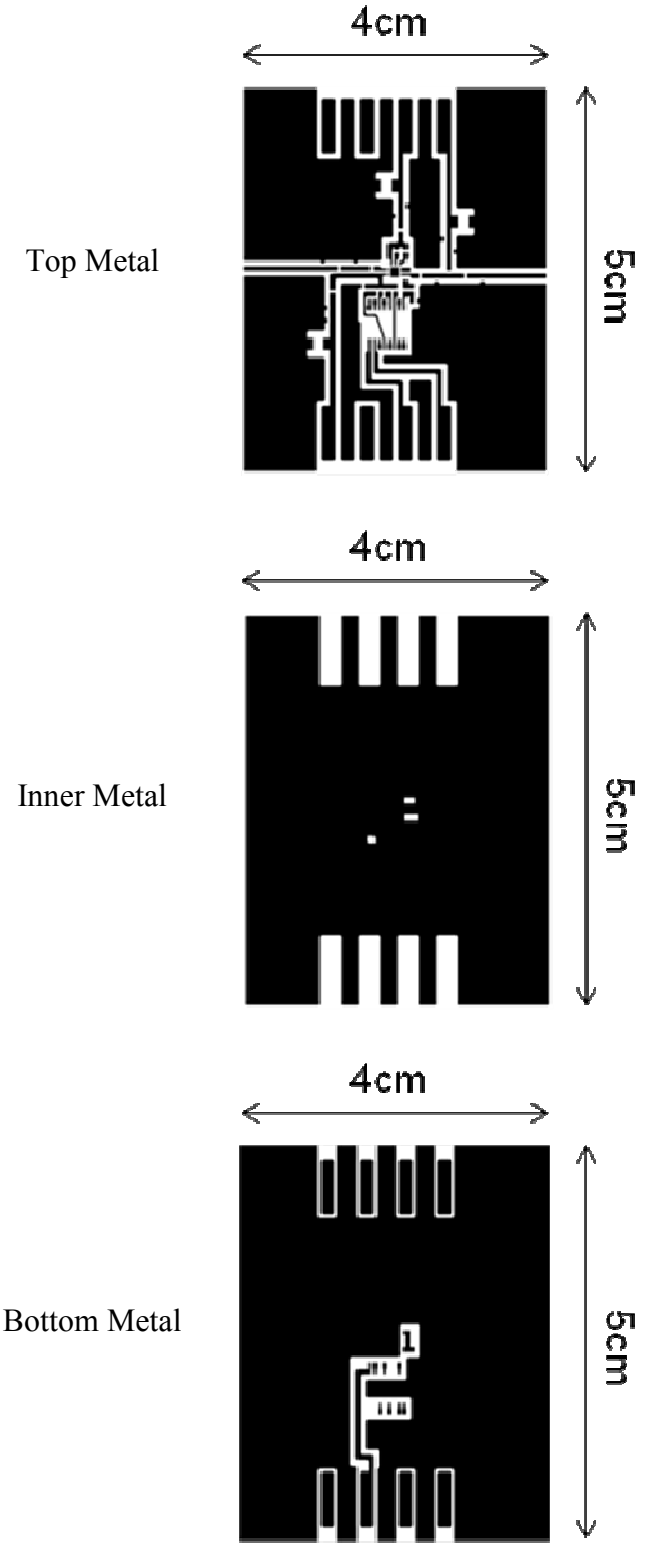


Figure C.1 TN_Prototype1 Fabrication Mask

(The printed mask is in real size dimension)

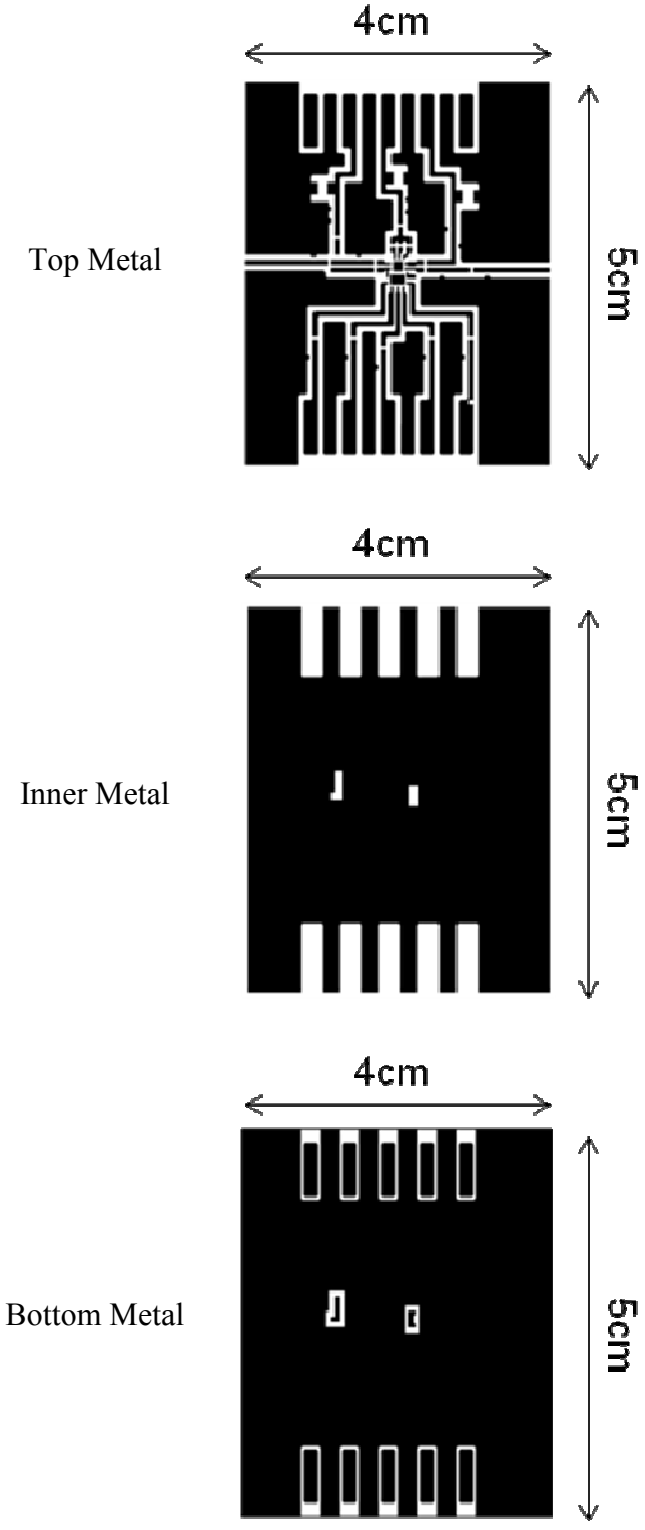


Figure C.2 TN_Prototype2 Fabrication Mask

(The printed mask is in real size dimension)

APPENDIX D

MMIC LAYOUT DESIGN

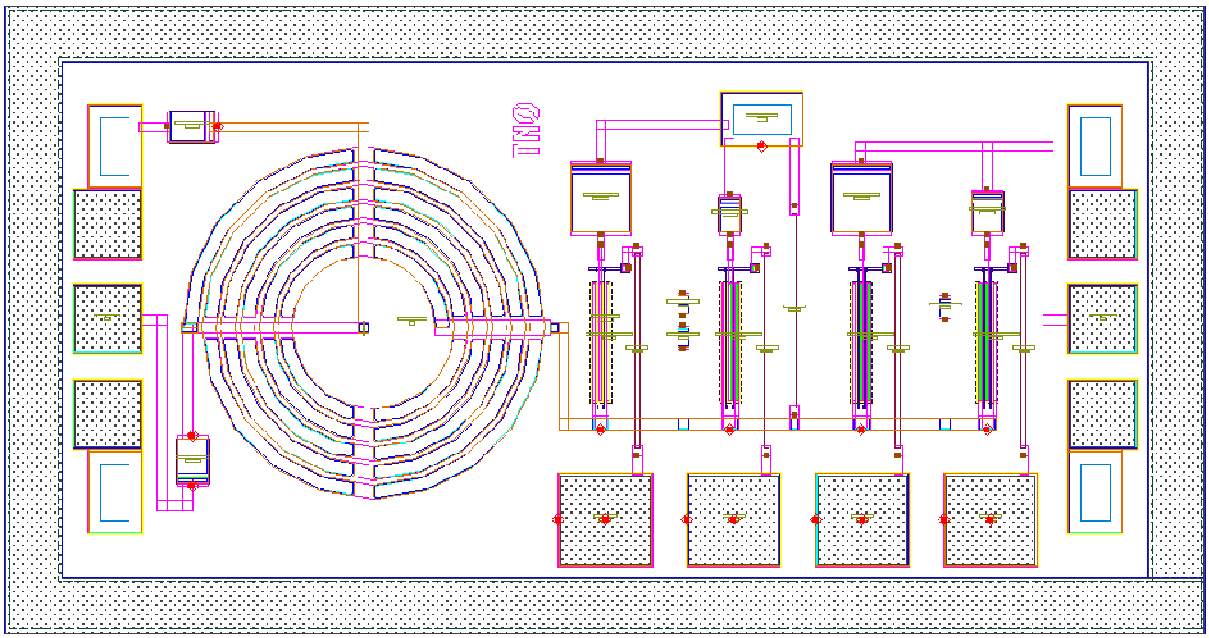


Figure D.1 TN0 Layout Design

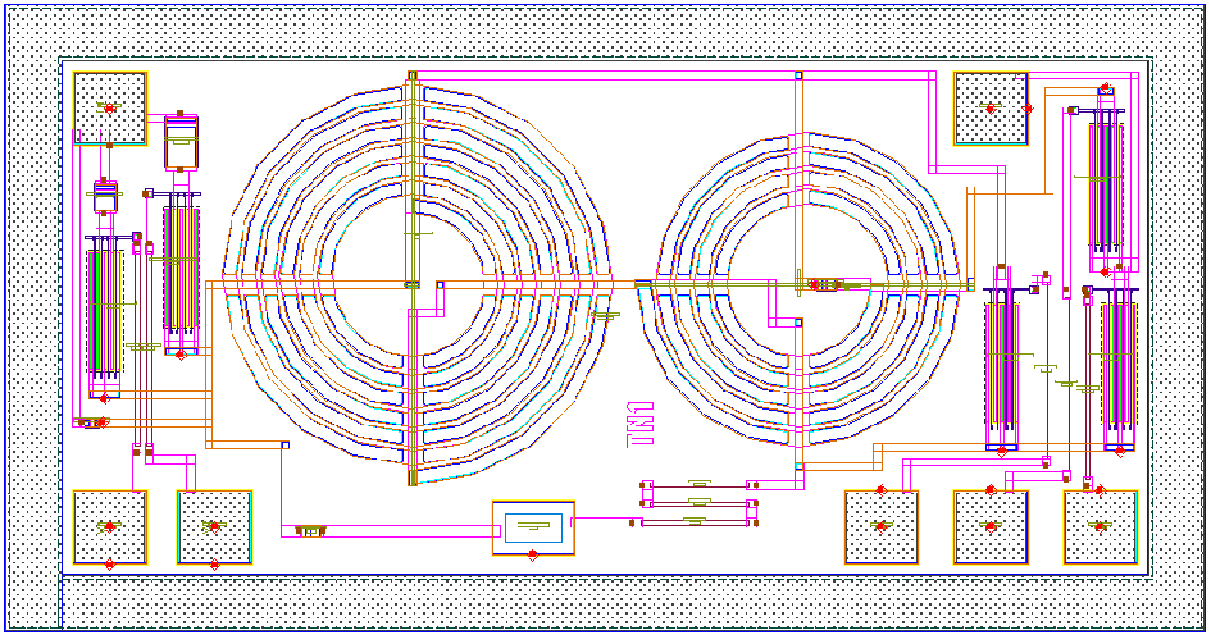


Figure D.2 TN1 Layout Design

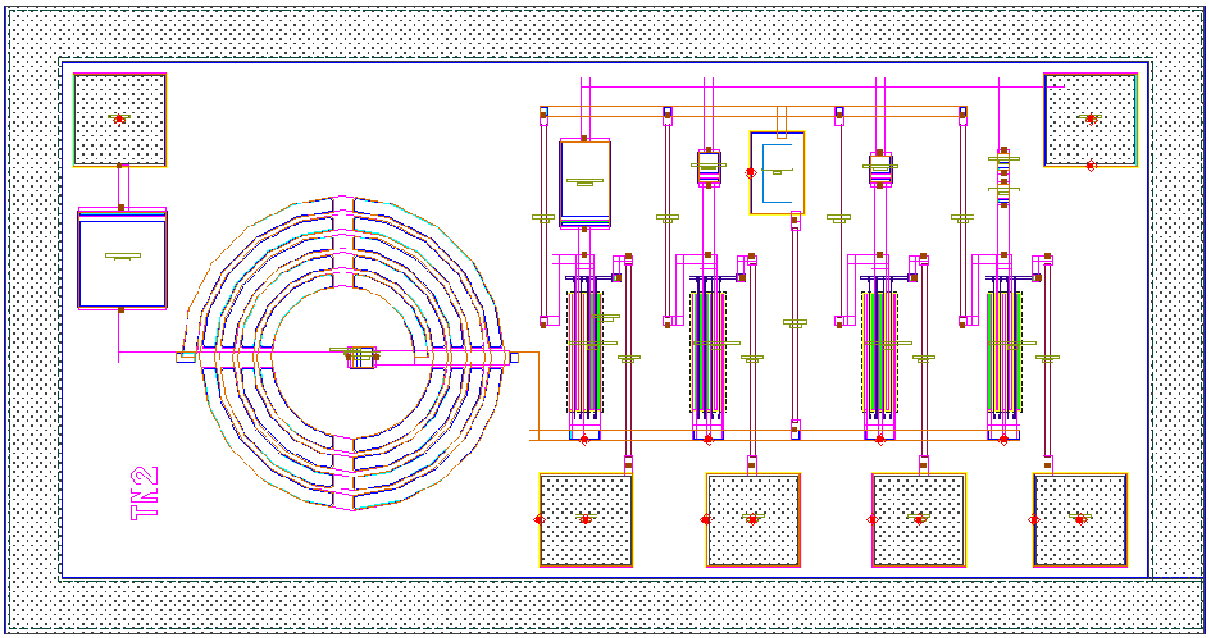


Figure D.3 TN2 Layout Design

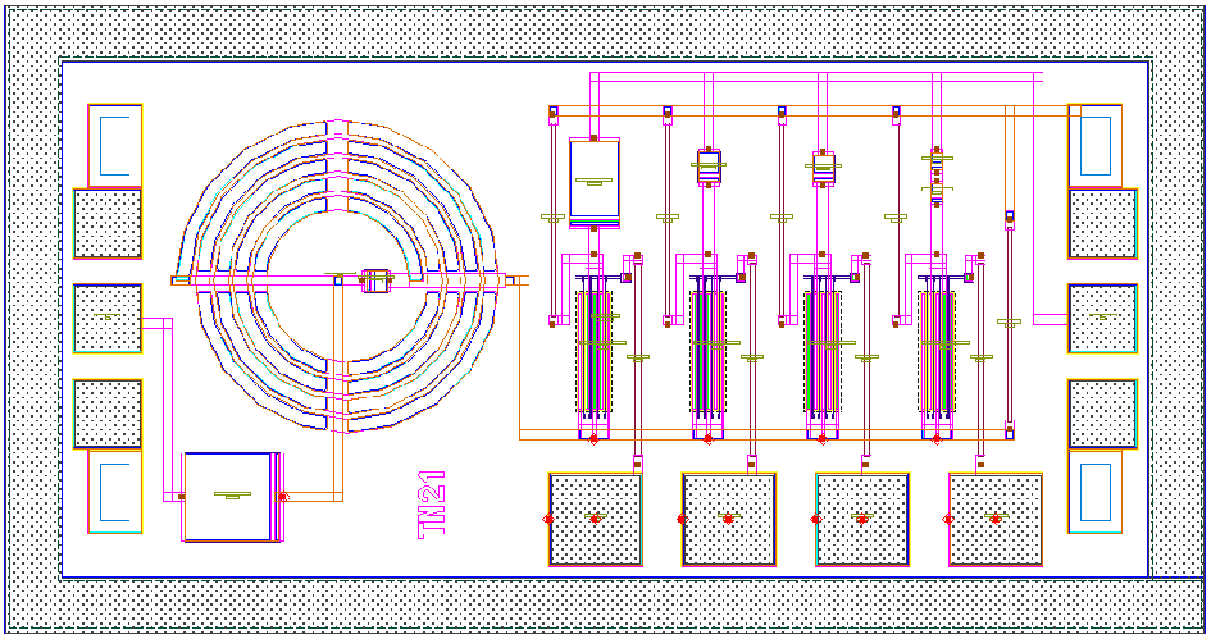


Figure D.4 TN21 Layout Design

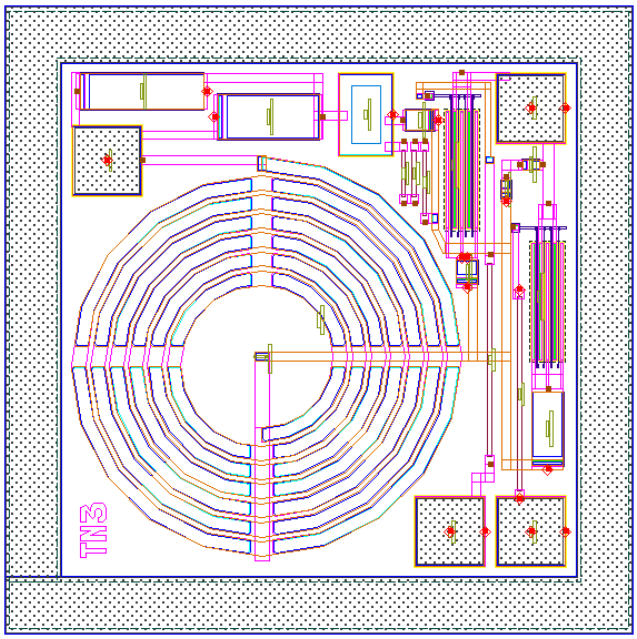


Figure D.5 TN3 Layout Design

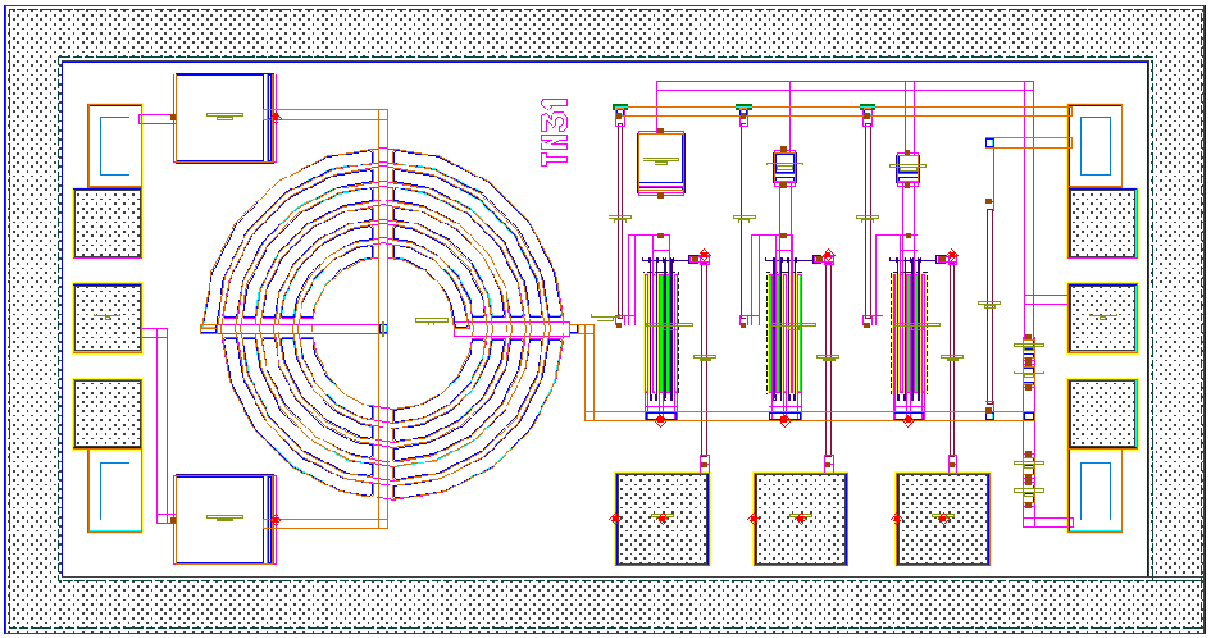


Figure D.6 TN31 Layout Design

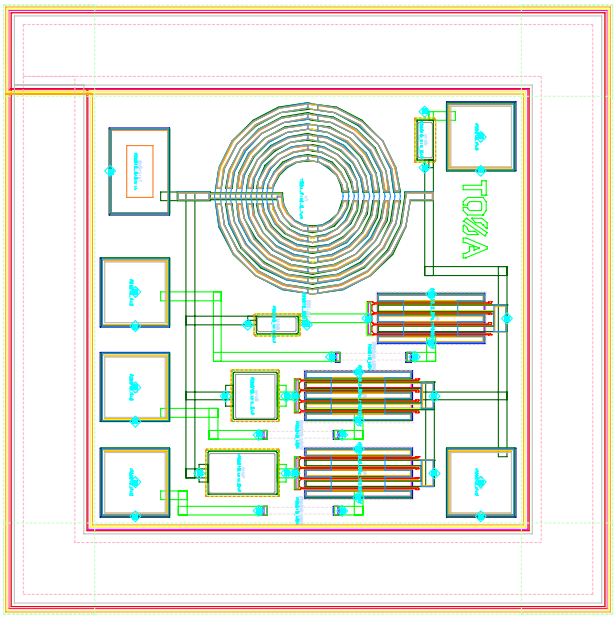


Figure D.7 TO0A Layout Design

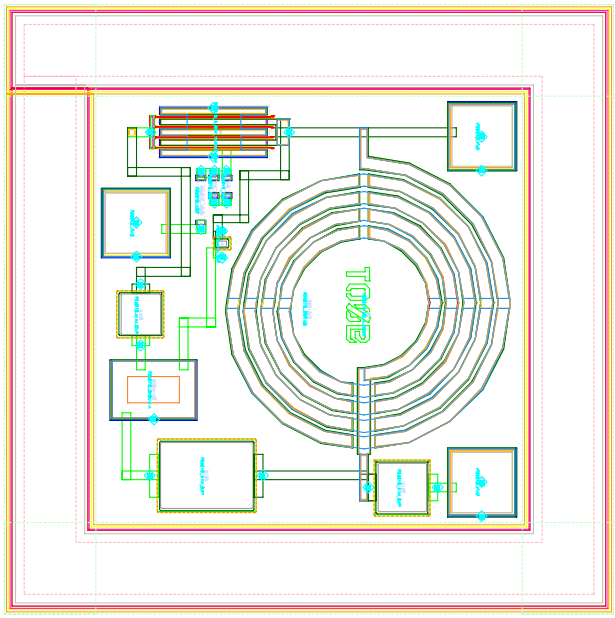


Figure D.8 TO0B Layout Design

The layout for circuit TO0 must be split into 2 die (TO0A and TO0B) due to limited wafer area and each die has the dimensions of 600 × 600 µm as shown in Figure D.7 and D.8. The fabricated dies were connected by wirebond between the bondpads.

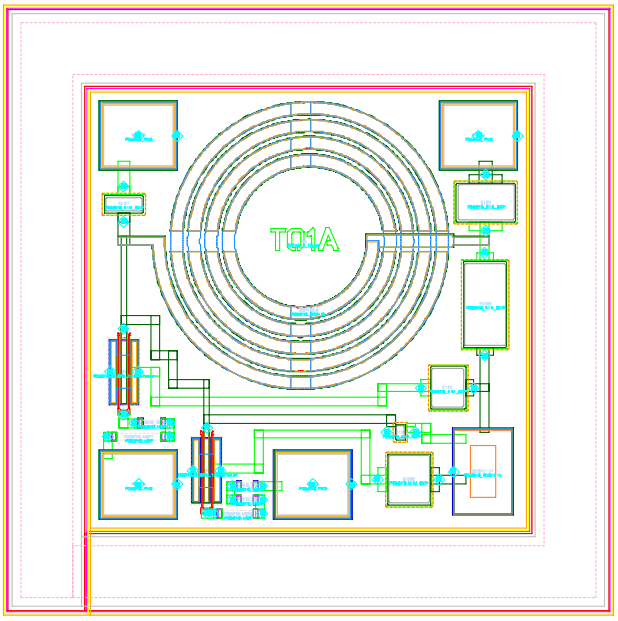


Figure D.9 TO1 Layout Design

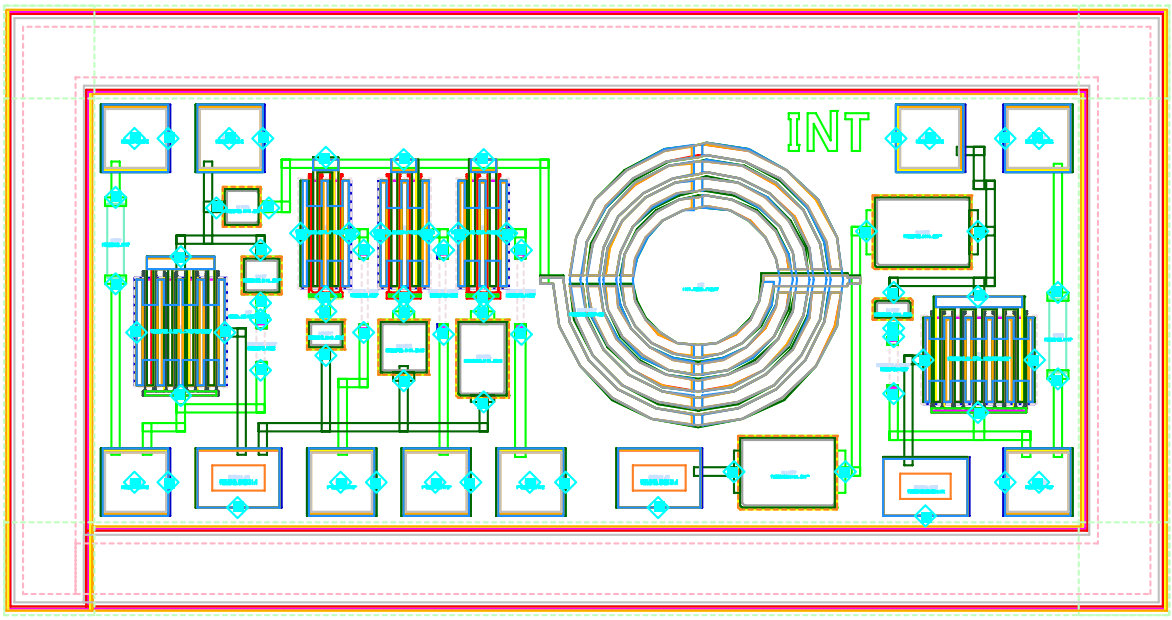


Figure D.10 INT Layout Design

APPENDIX E

WIREBOND DIAGRAM

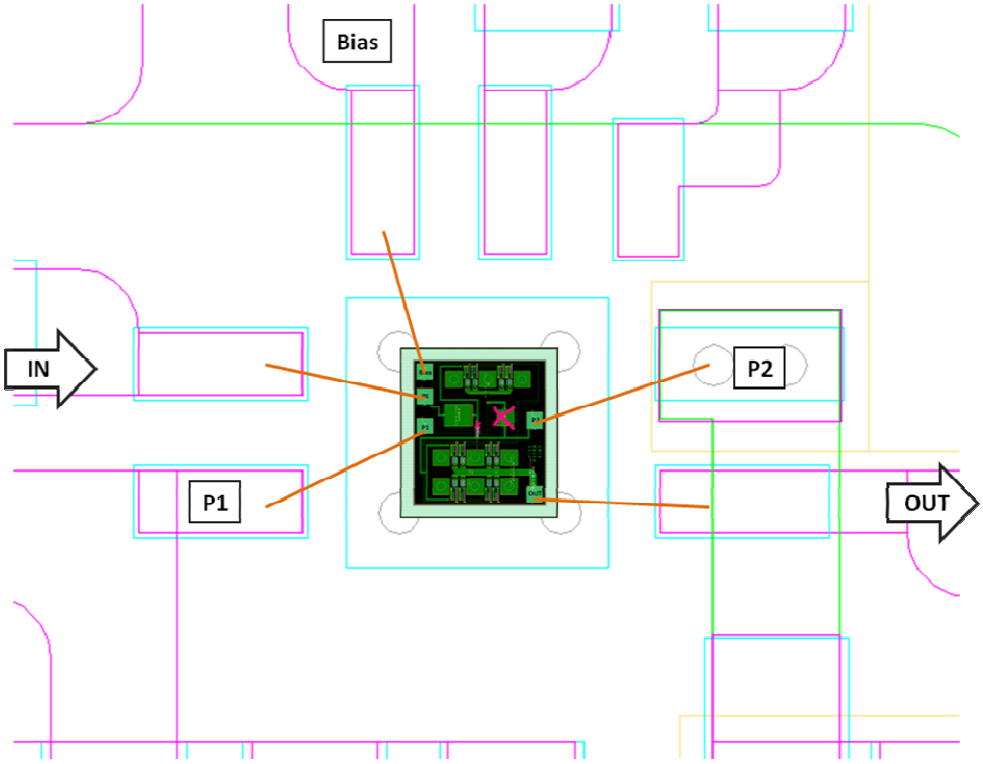


Figure E.1 DTN1 Wirebond Diagram

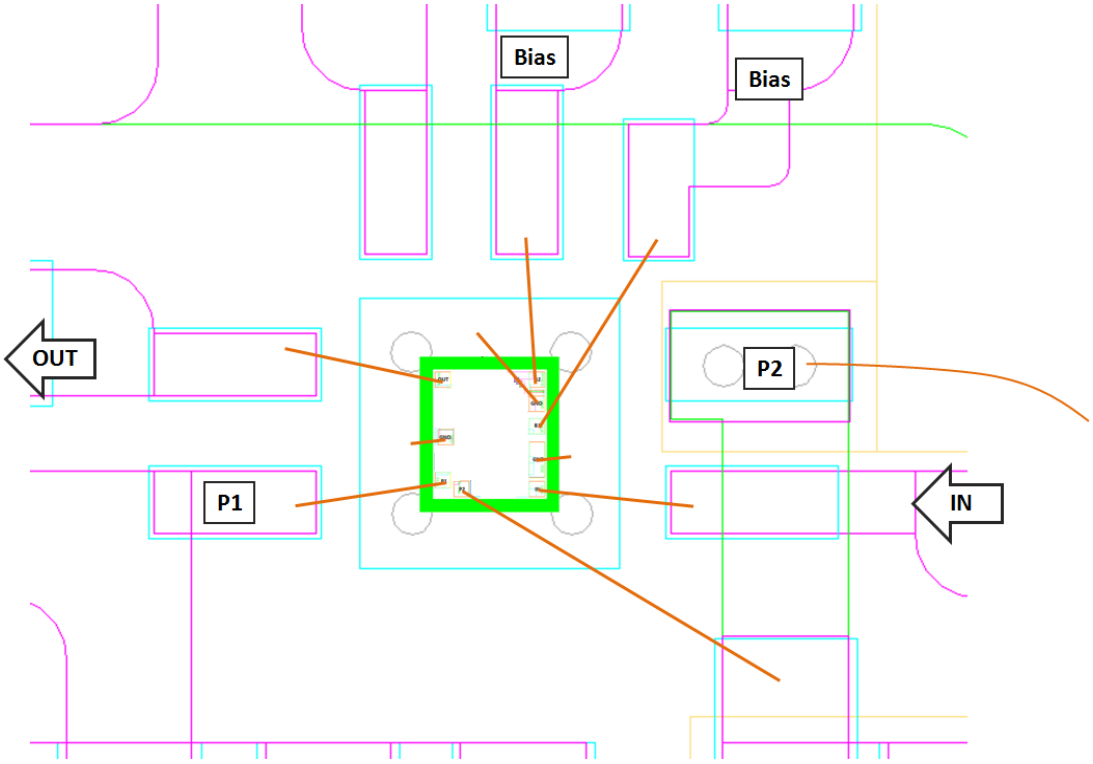


Figure E.2 DTN2 & DTN3 Wirebond Diagram

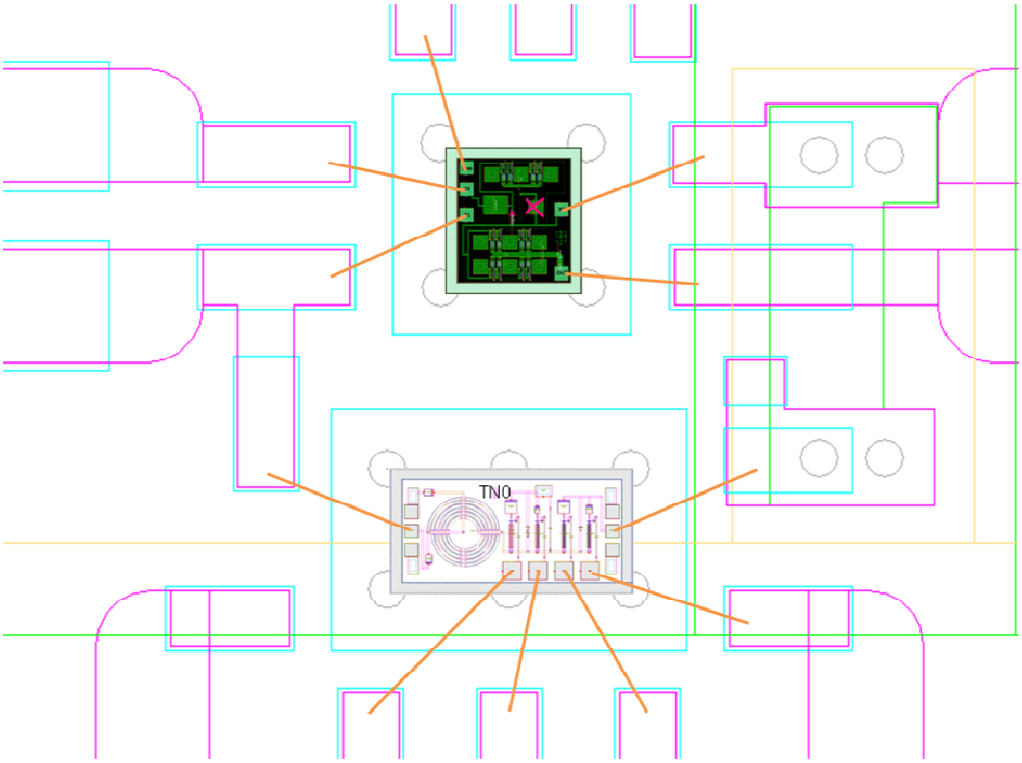


Figure E.3 TN0 Wirebond Diagram

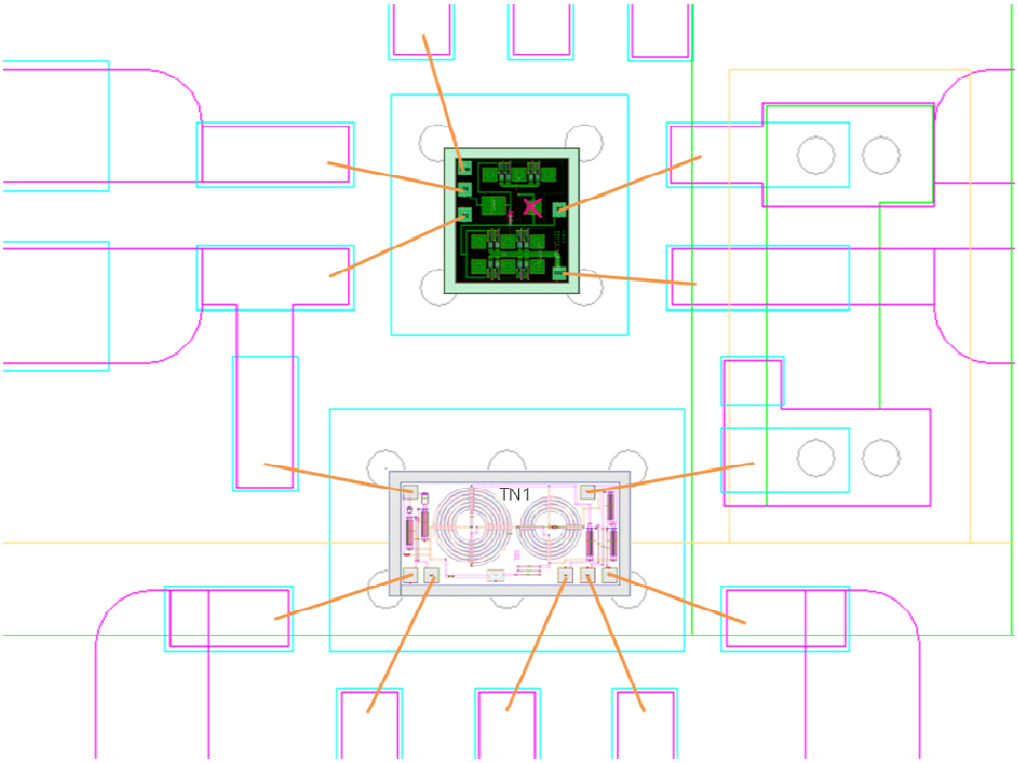


Figure E.4 TN1 Wirebond Diagram

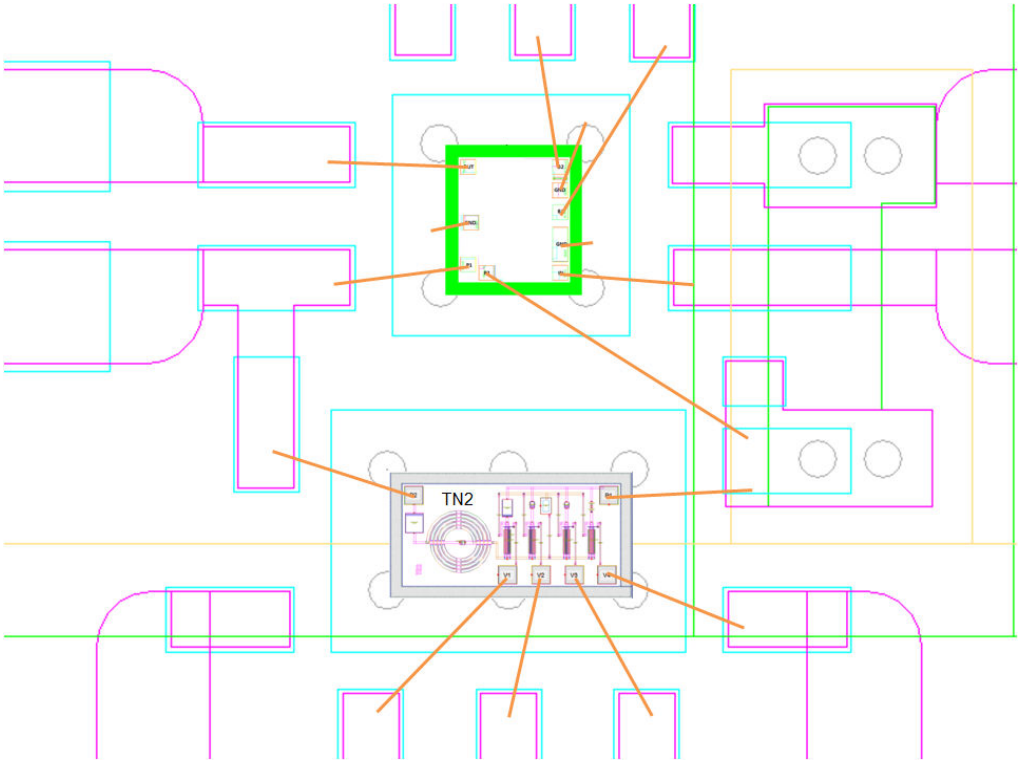


Figure E.5 TN2 Wirebond Diagram

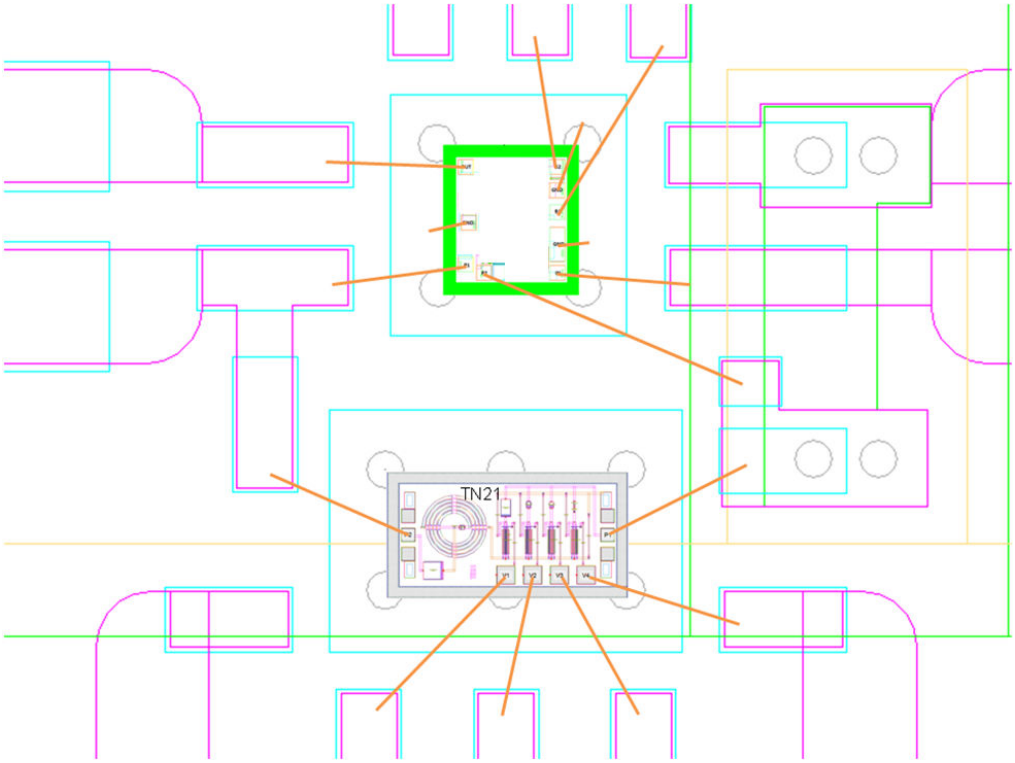


Figure E.6 TN21 Wirebond Diagram

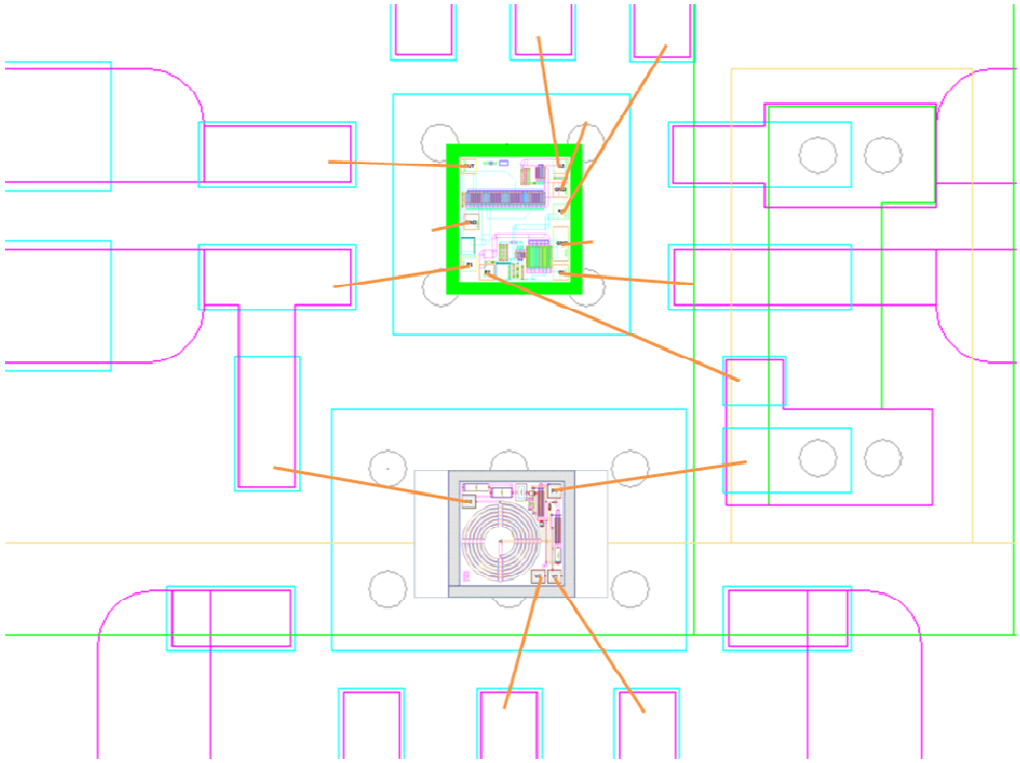


Figure E.7 TN3 Wirebond Diagram

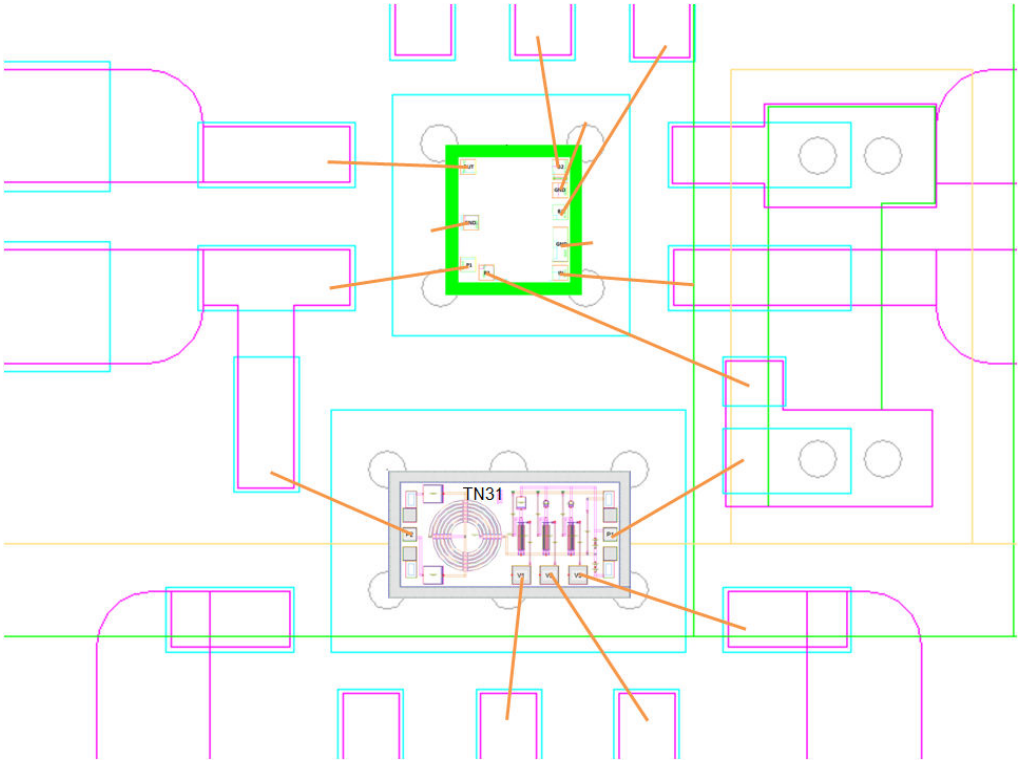


Figure E.8 TN31 Wirebond Diagram

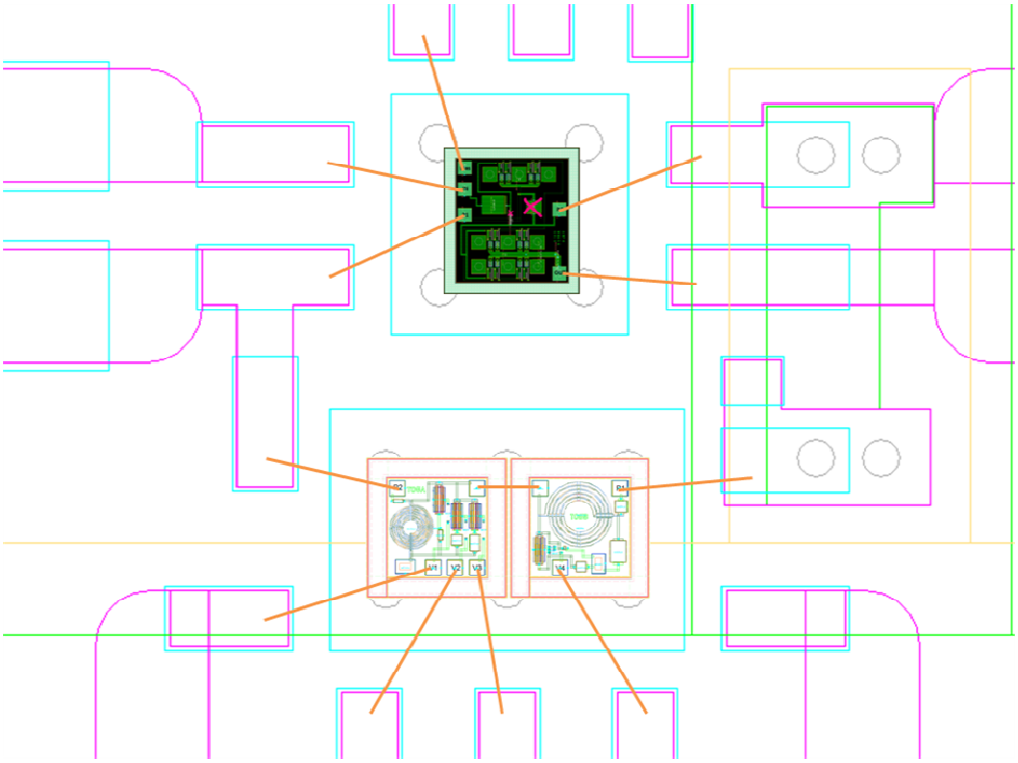


Figure E.9 TO0A & TO0B Wirebond Diagram

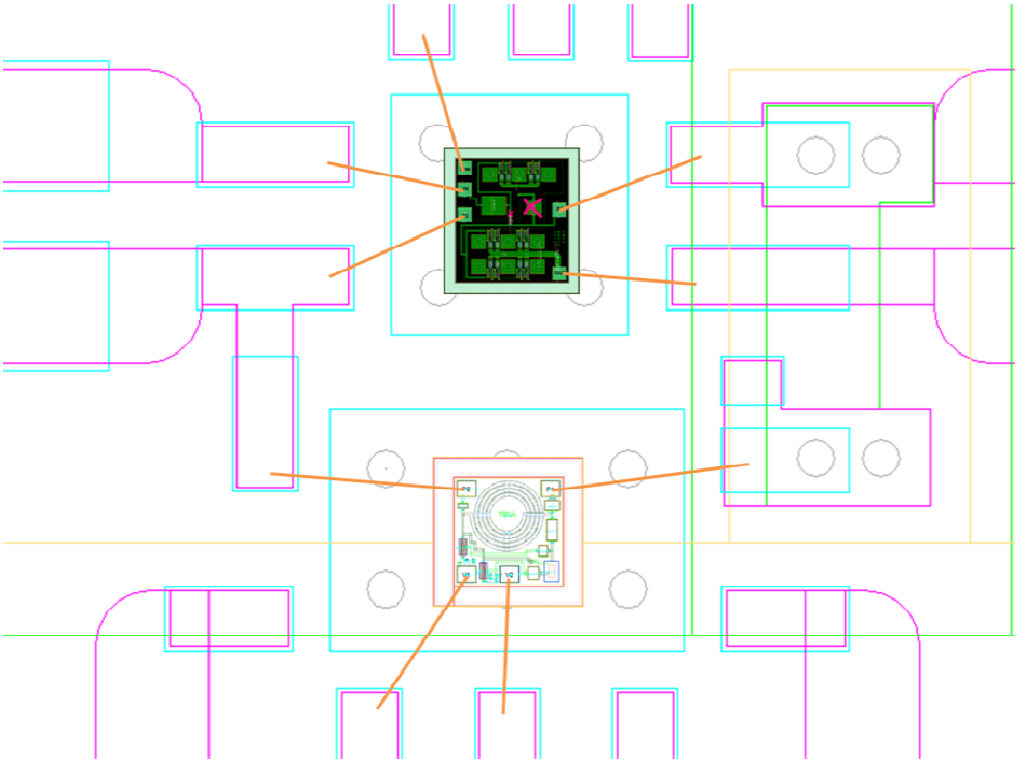


Figure E.10 TO1 Wirebond Diagram

APPENDIX F

BOARD POPULATION DIAGRAM

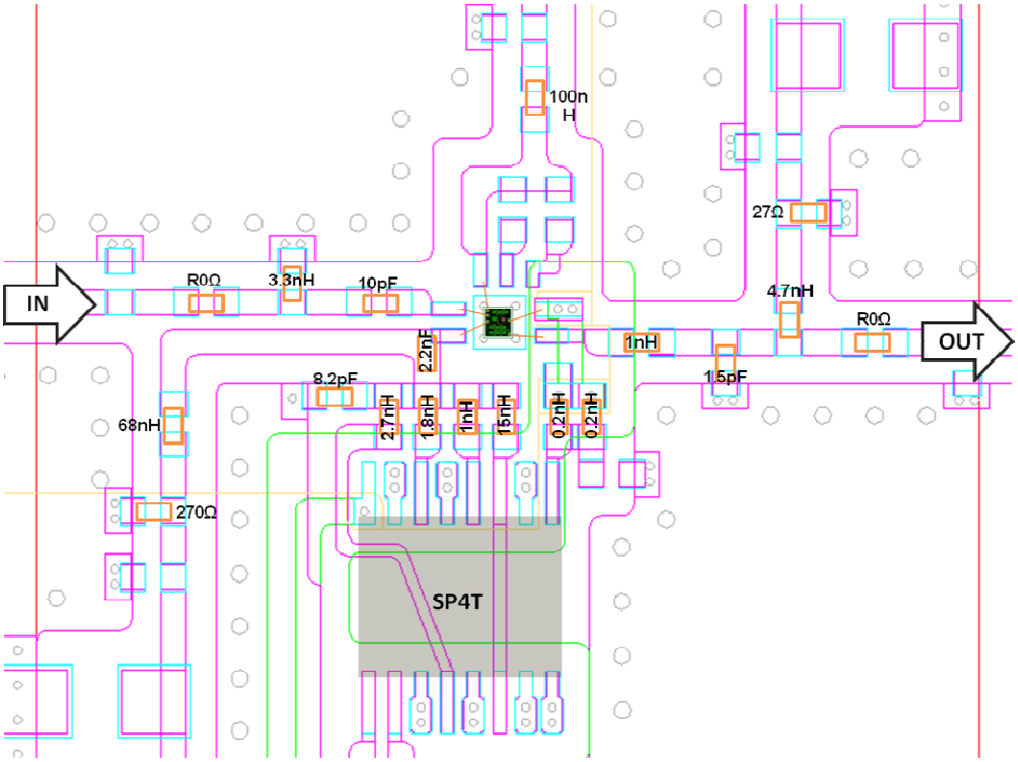


Figure F.1 DTN1 Board Population Diagram

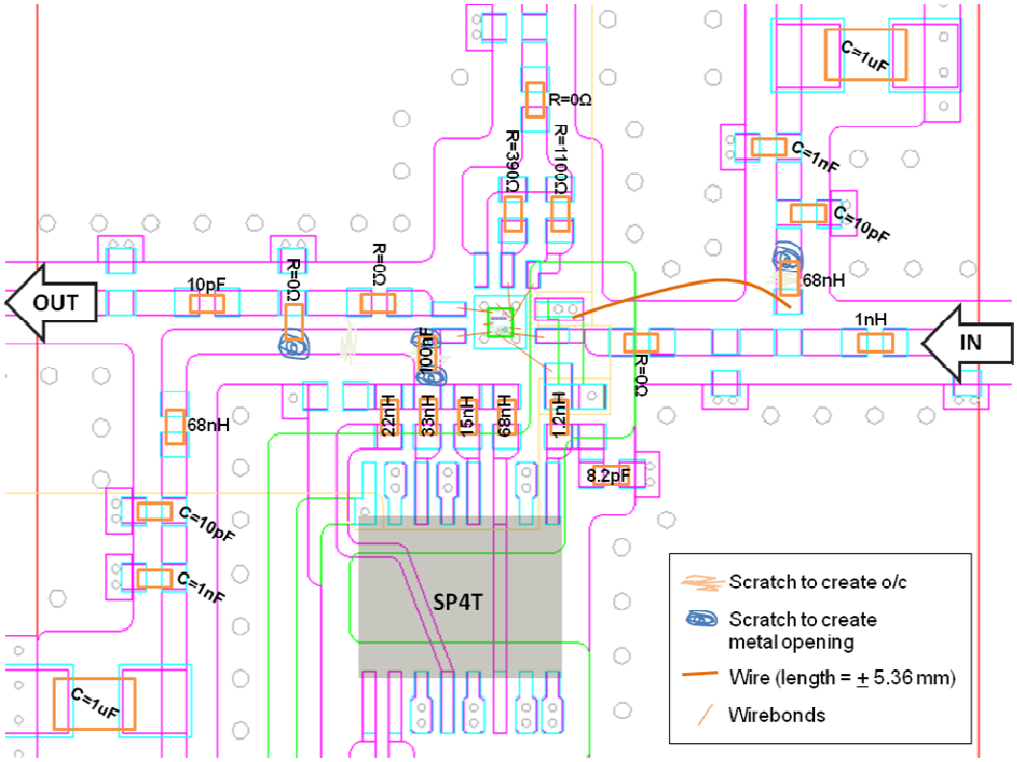


Figure F.2 DTN2 Board Population Diagram

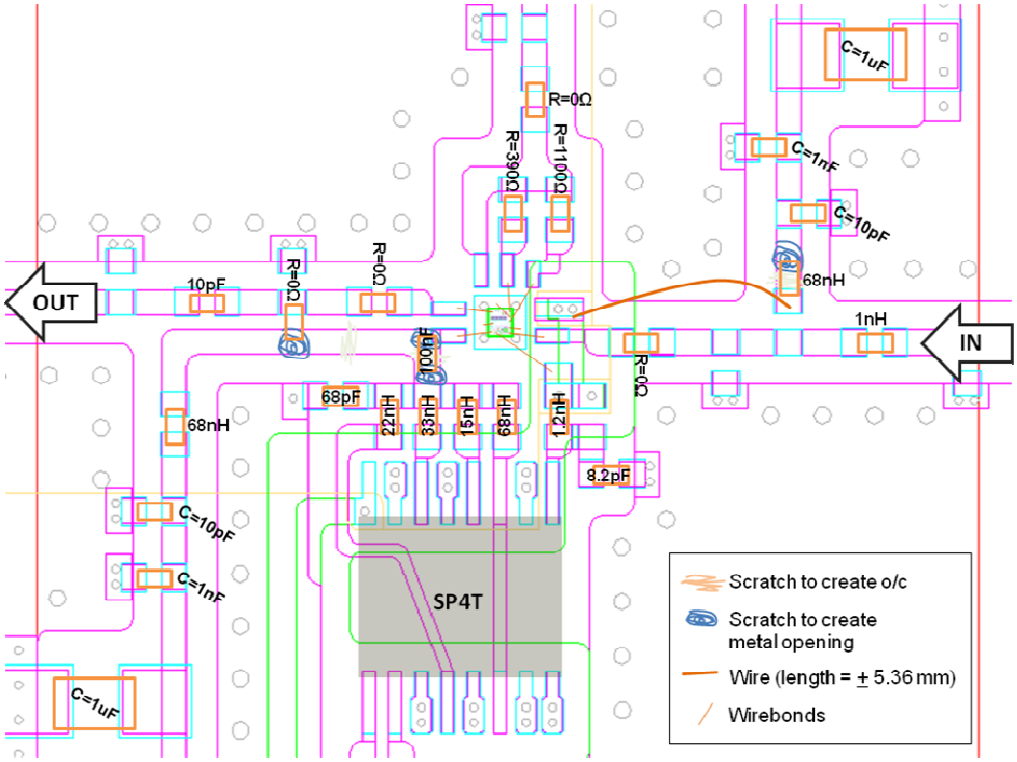


Figure F.3 DTN3 Board Population Diagram

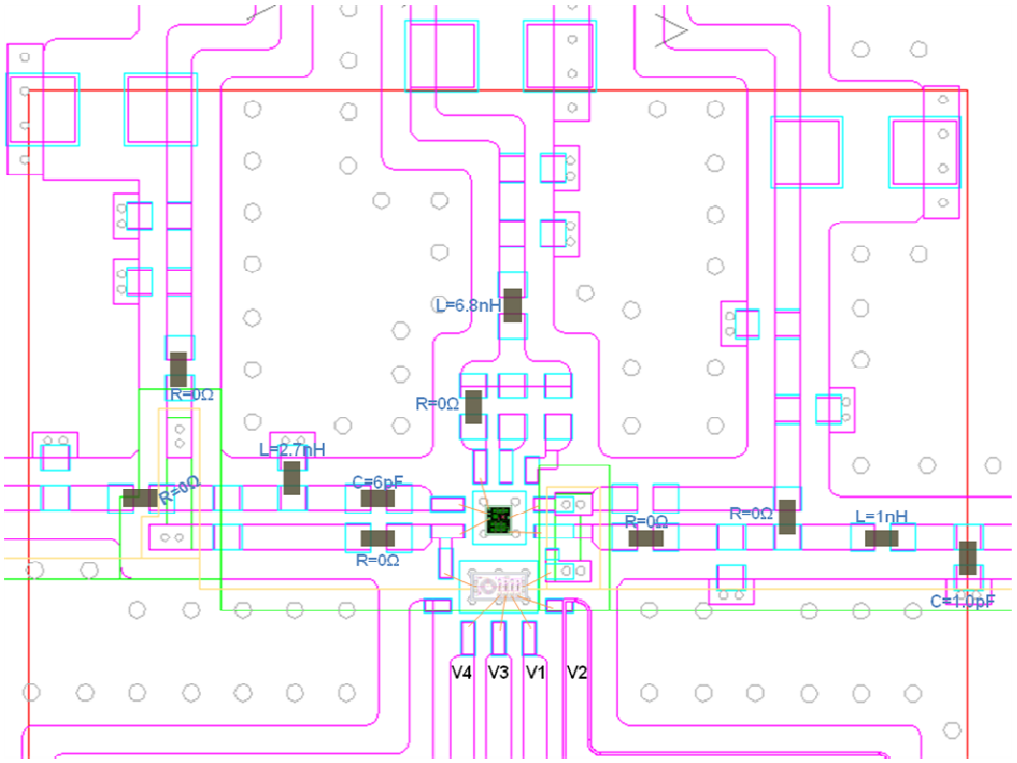


Figure F.4 TN0 Board Population Diagram

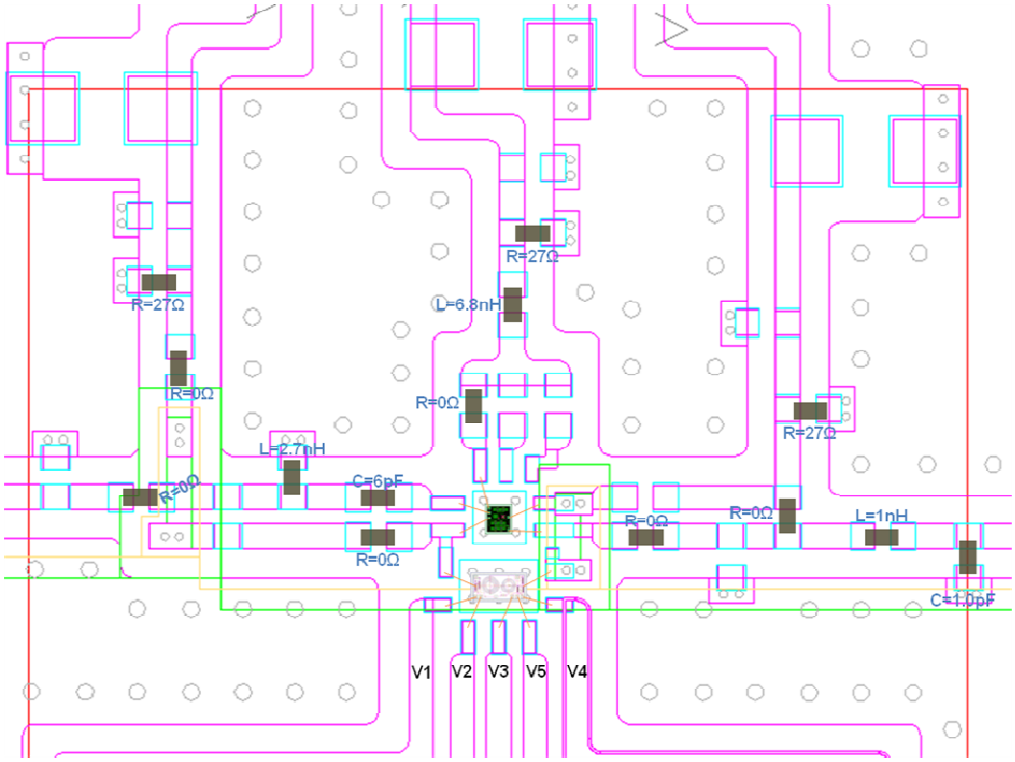


Figure F.5 TN1 Board Population Diagram

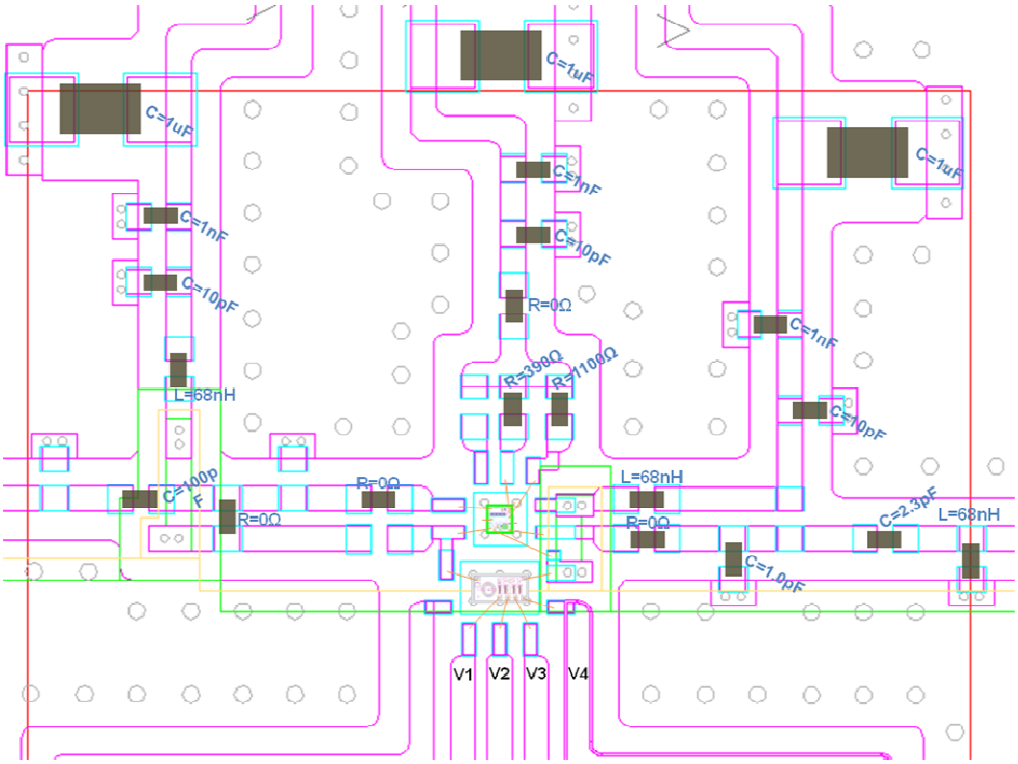


Figure F.6 TN2 Board Population Diagram

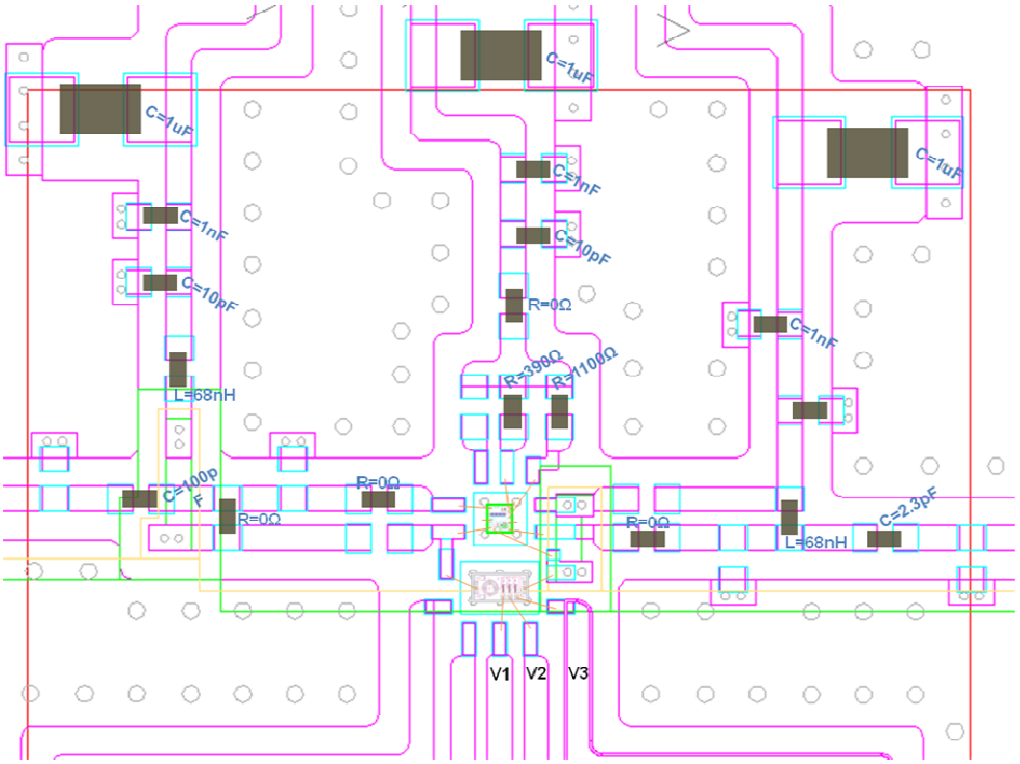


Figure F.7 TN31 Board Population Diagram

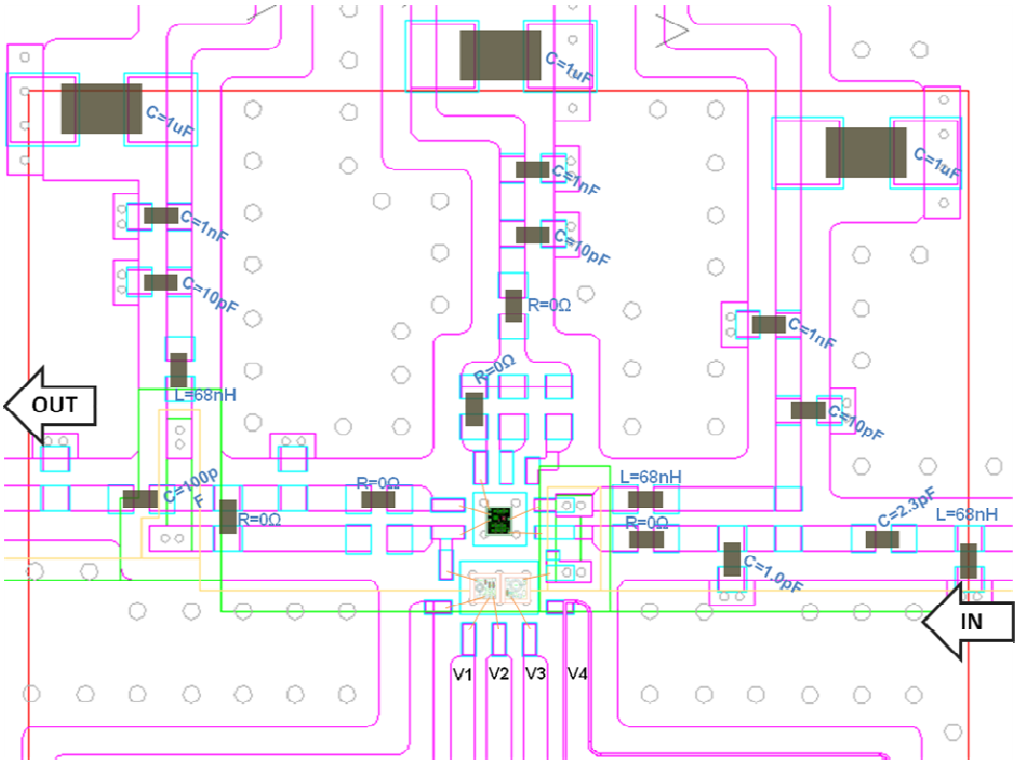


Figure F.8 TO0A & TO0B Board Population Diagram

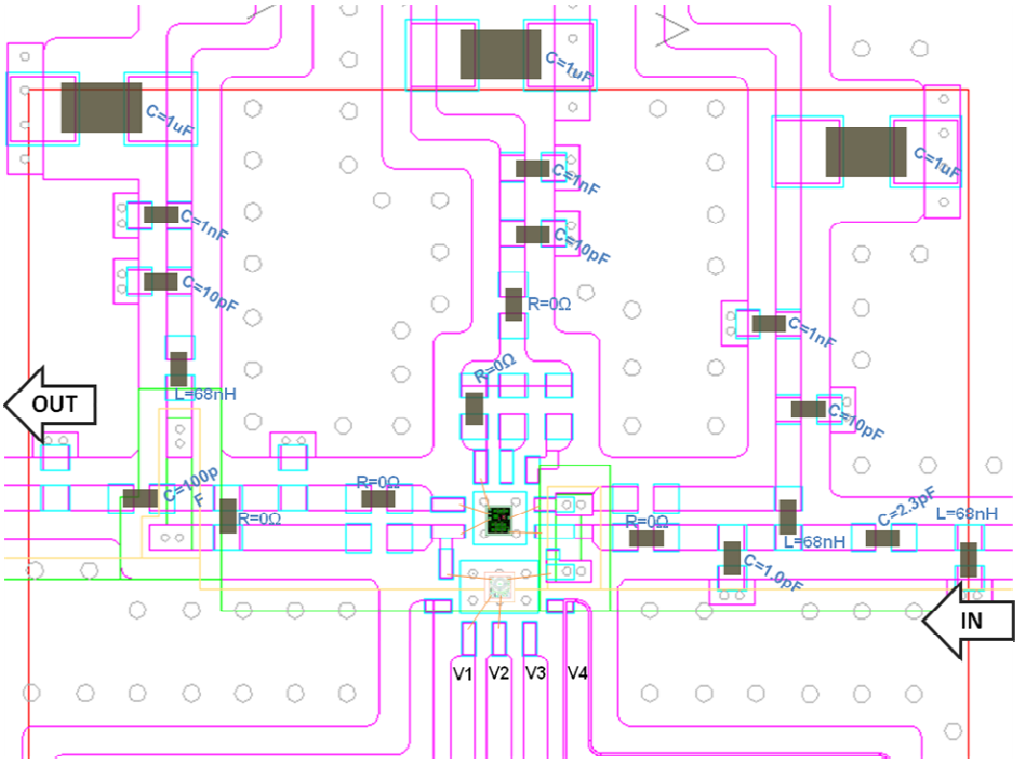


Figure F.9 TO1 Board Population Diagram

APPENDIX G

DC BIASING DIAGRAM

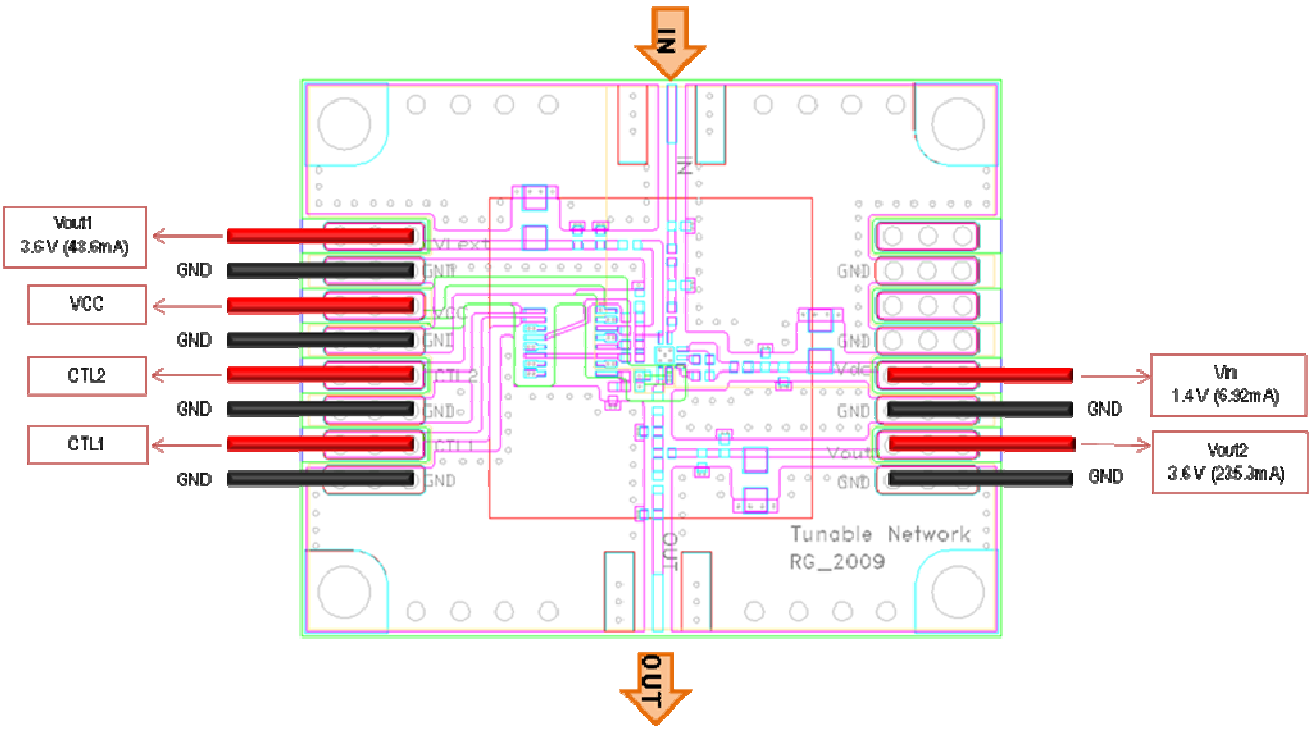


Figure G.1 DTN1 DC Biasing Diagram

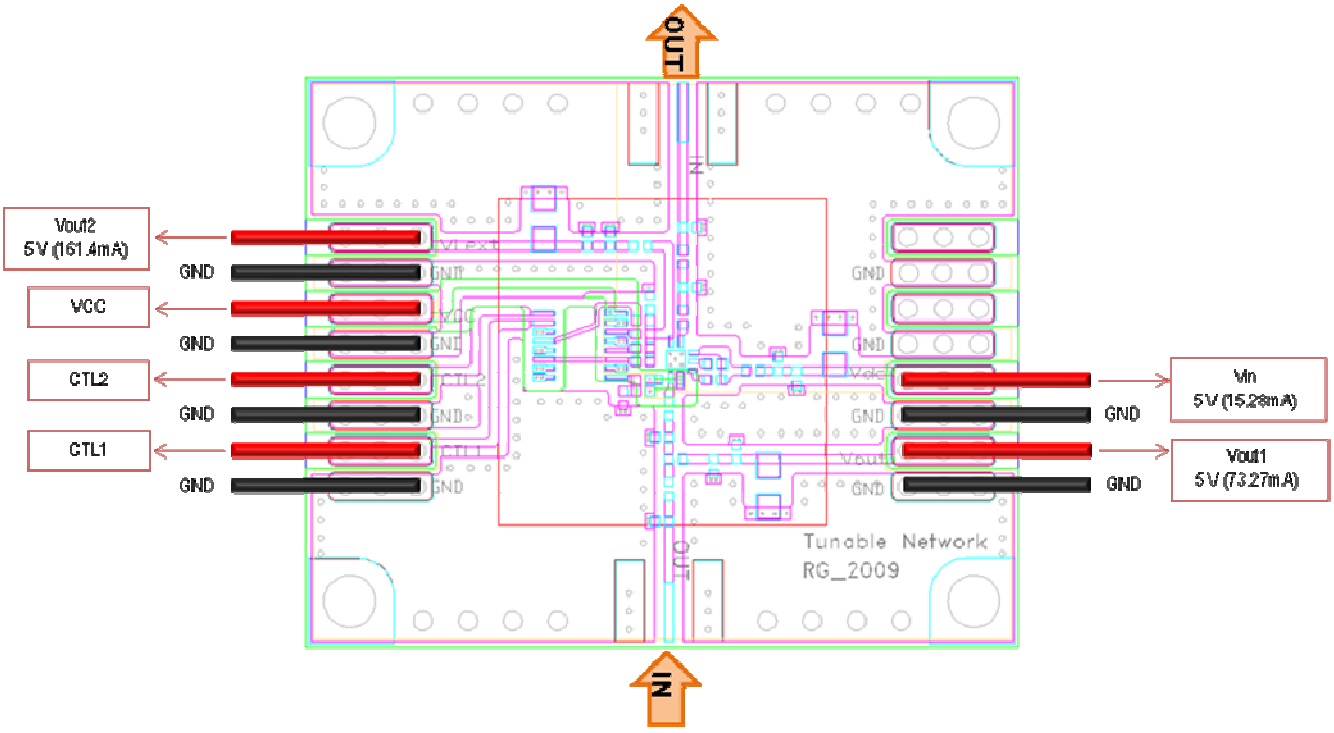


Figure G.2 DTN2 & DTN3 DC Biasing Diagram

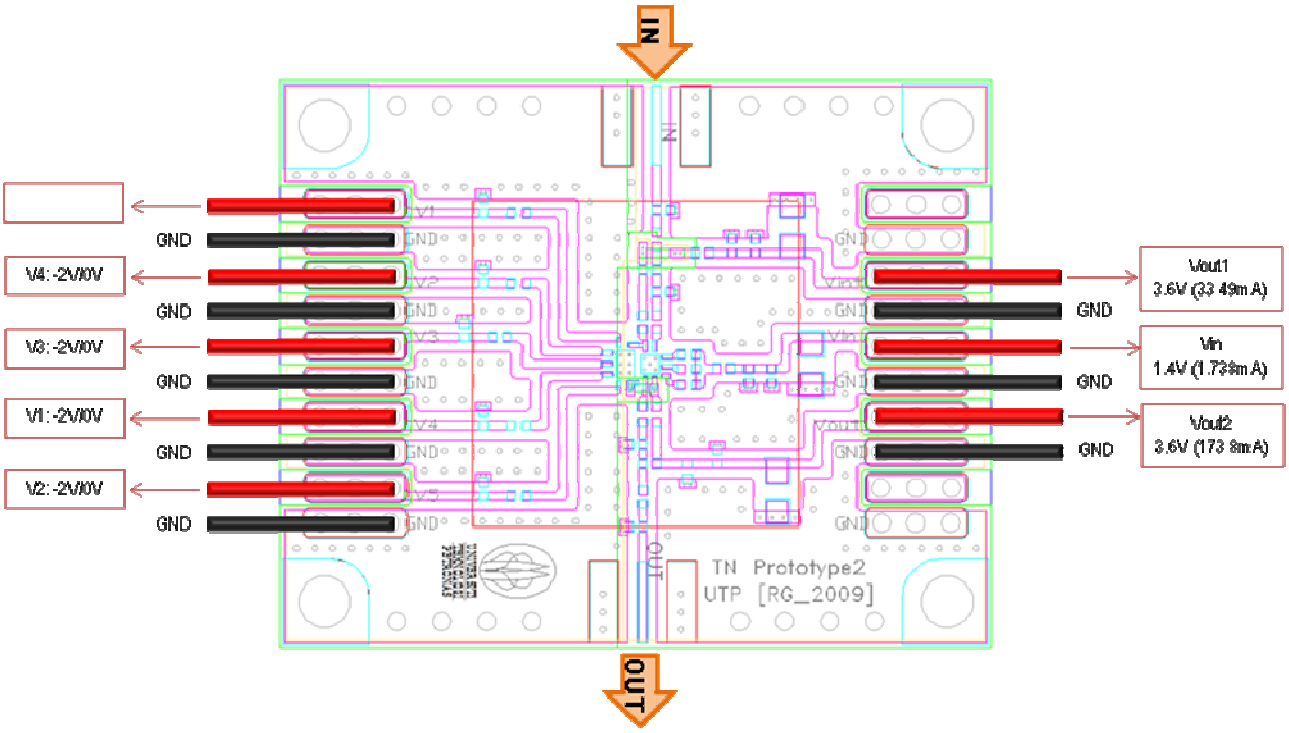


Figure G.3 TN0 DC Biasing Diagram

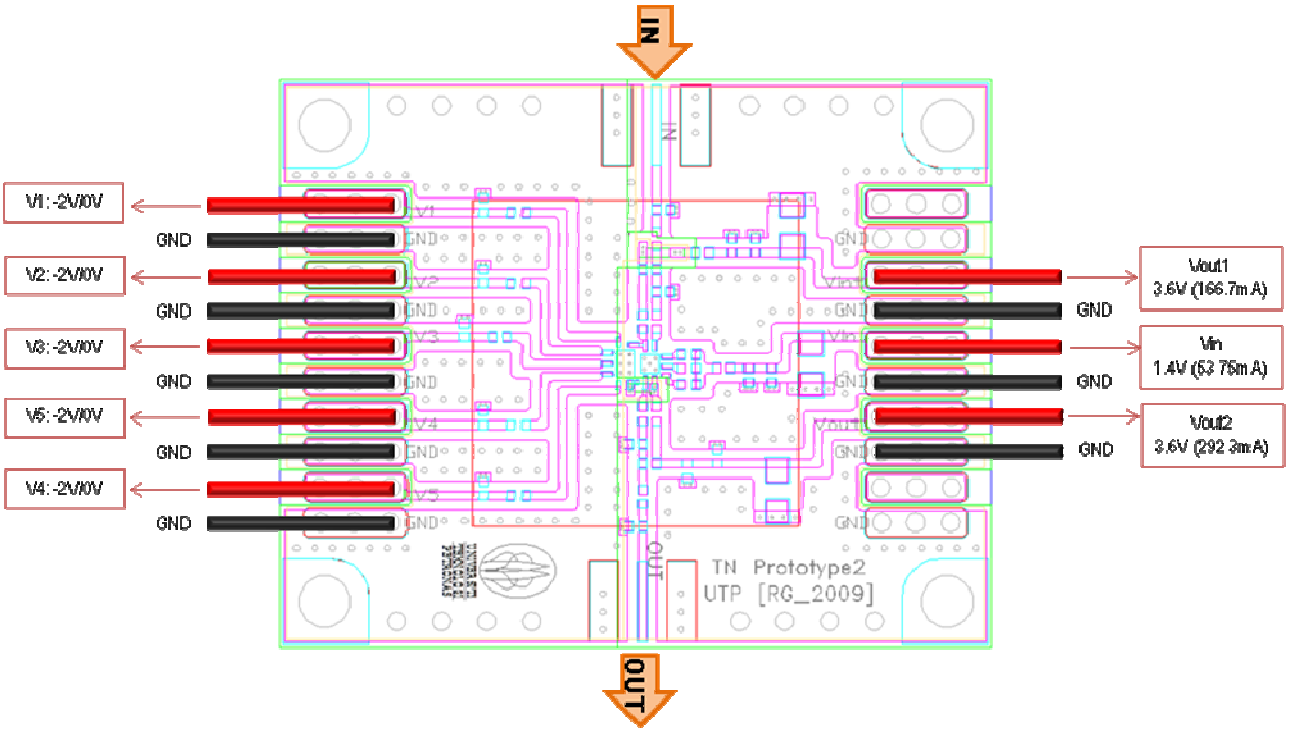


Figure G.4 TN1 DC Biasing Diagram

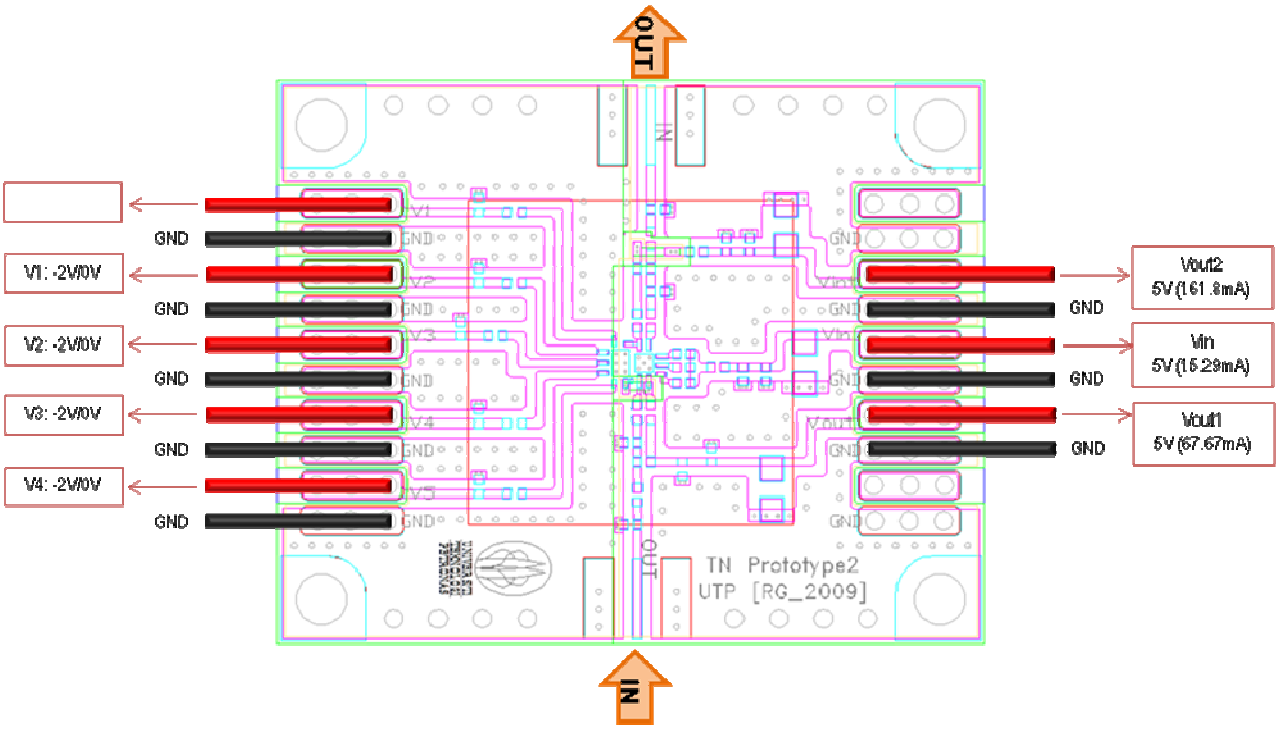


Figure G.5 TN2 DC Biasing Diagram

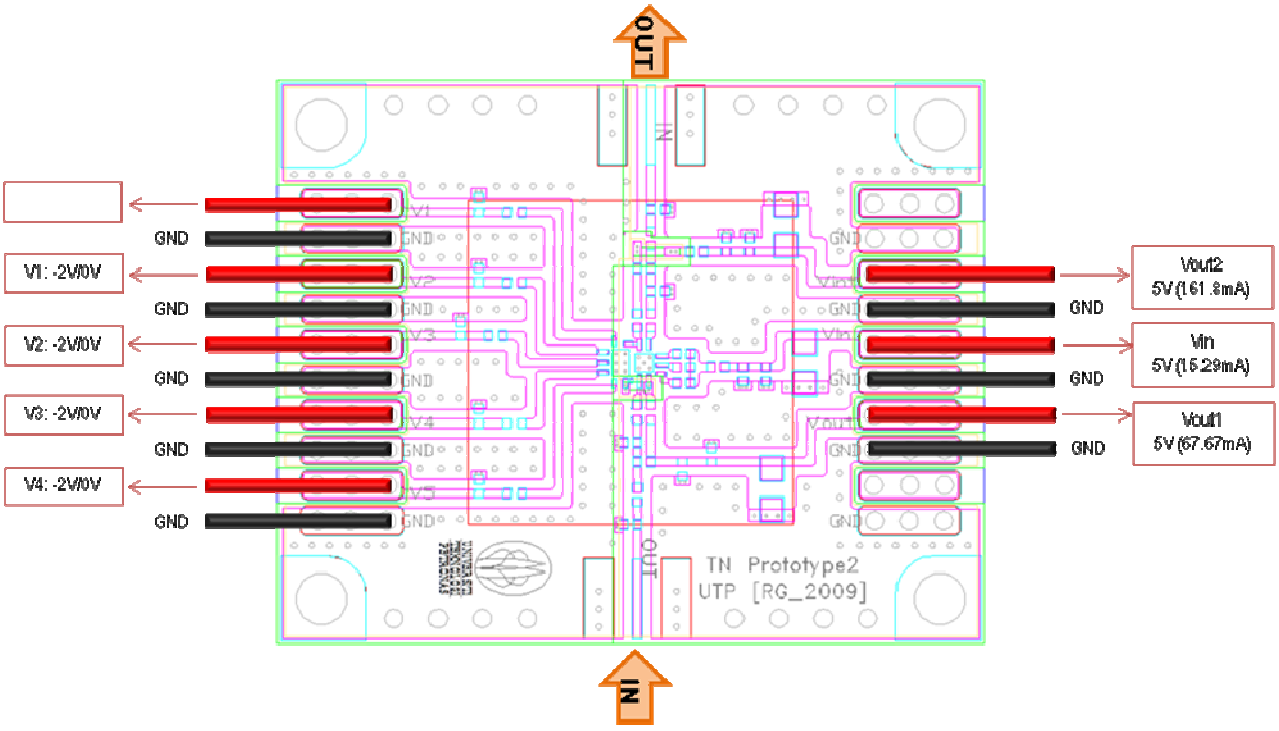


Figure G.6 TN21 DC Biasing Diagram

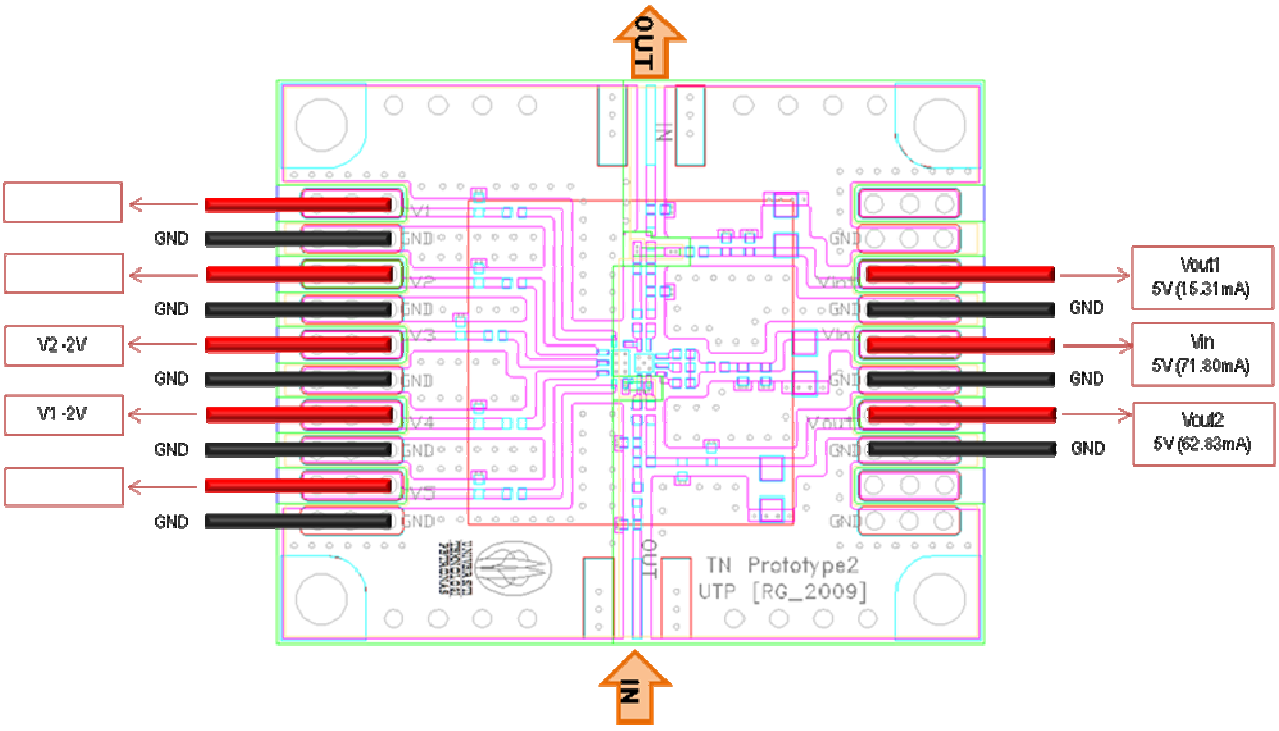


Figure G.7 TN3 DC Biasing Diagram

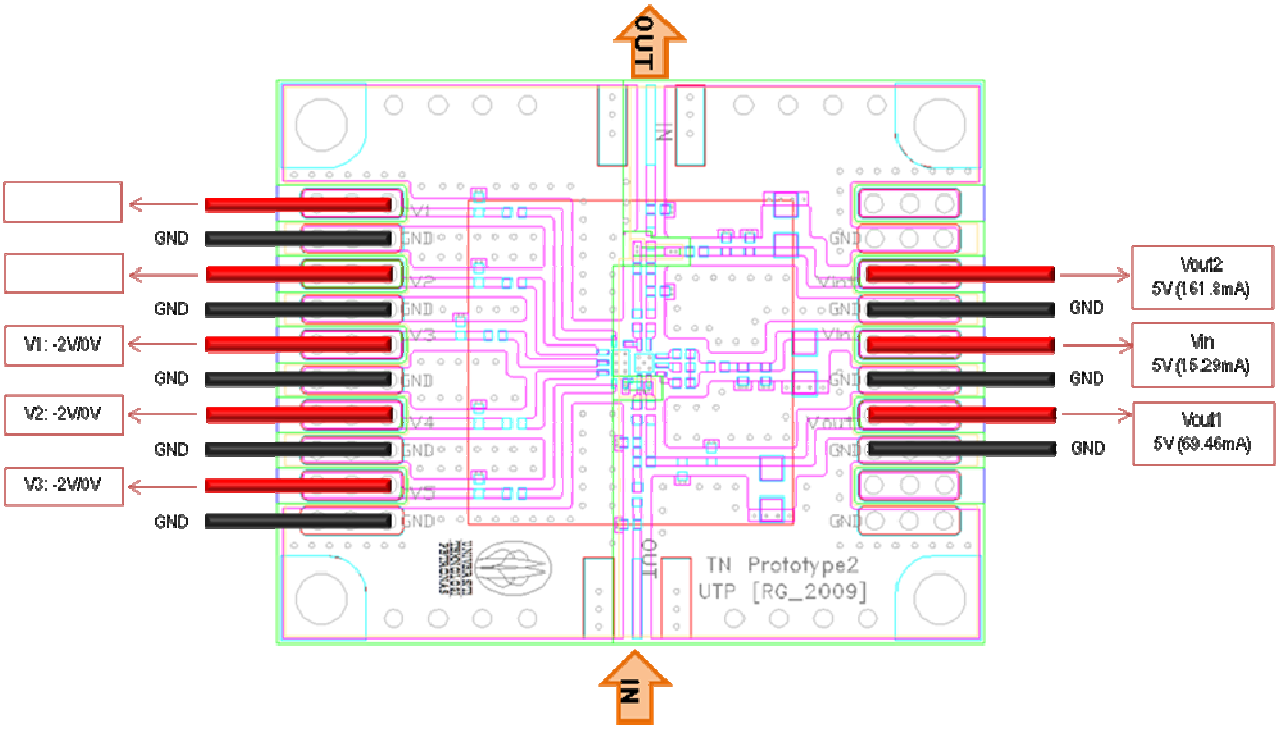


Figure G.8 TN31 DC Biasing Diagram

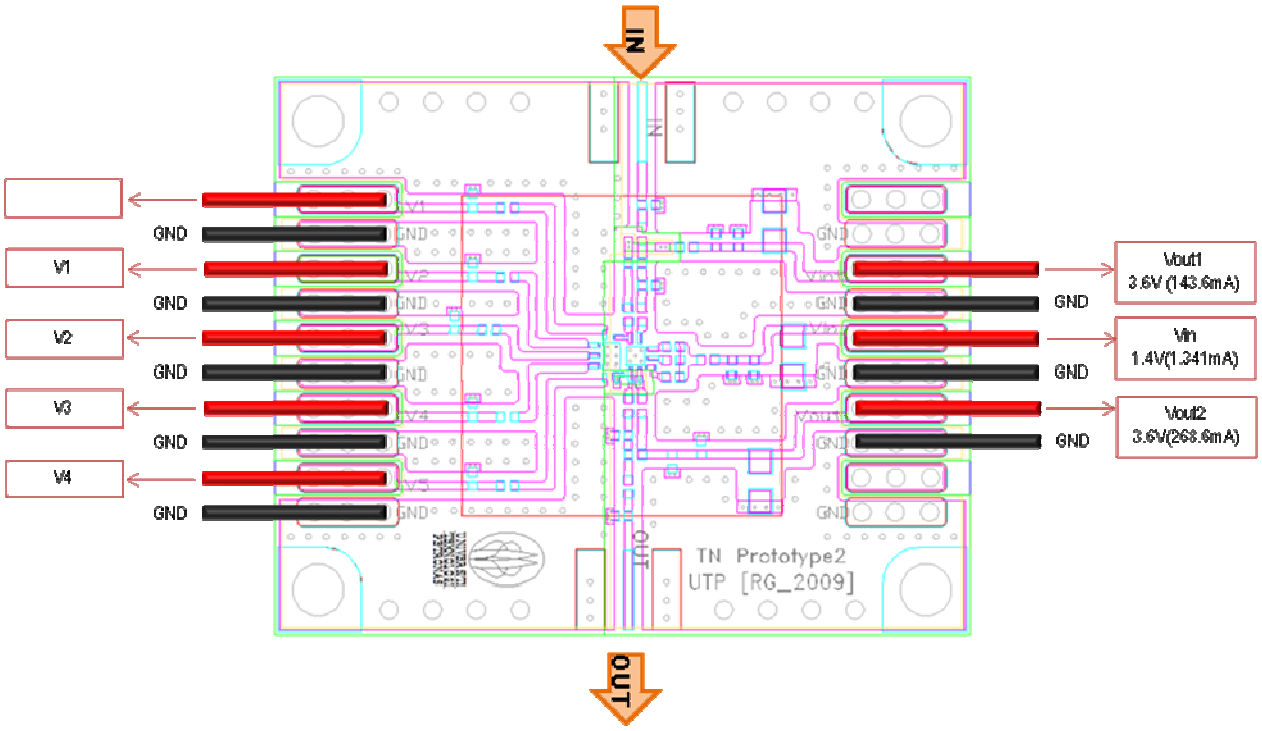


Figure G.9 TO0A & TO0B DC Biasing Diagram

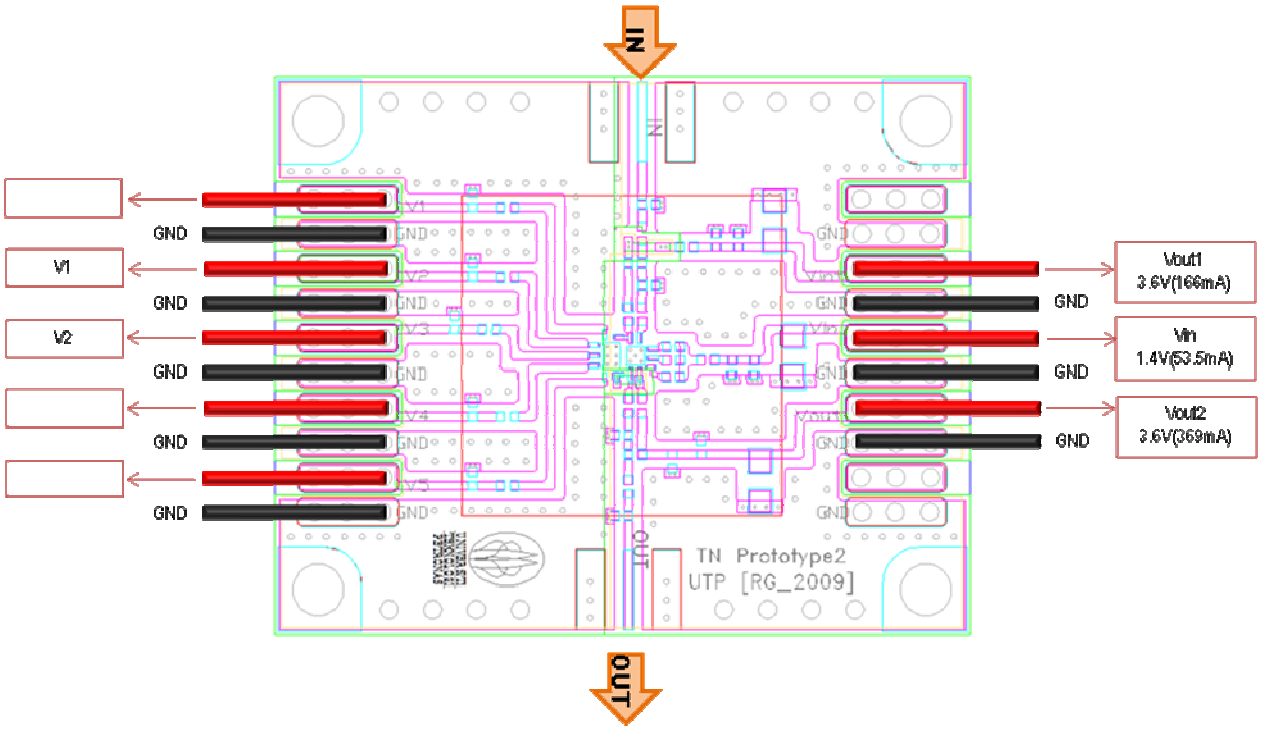


Figure G.10 TO1 DC Biasing Diagram

APPENDIX H

PROTOTYPE BOARD LAYOUT ON EM-SIMULATOR

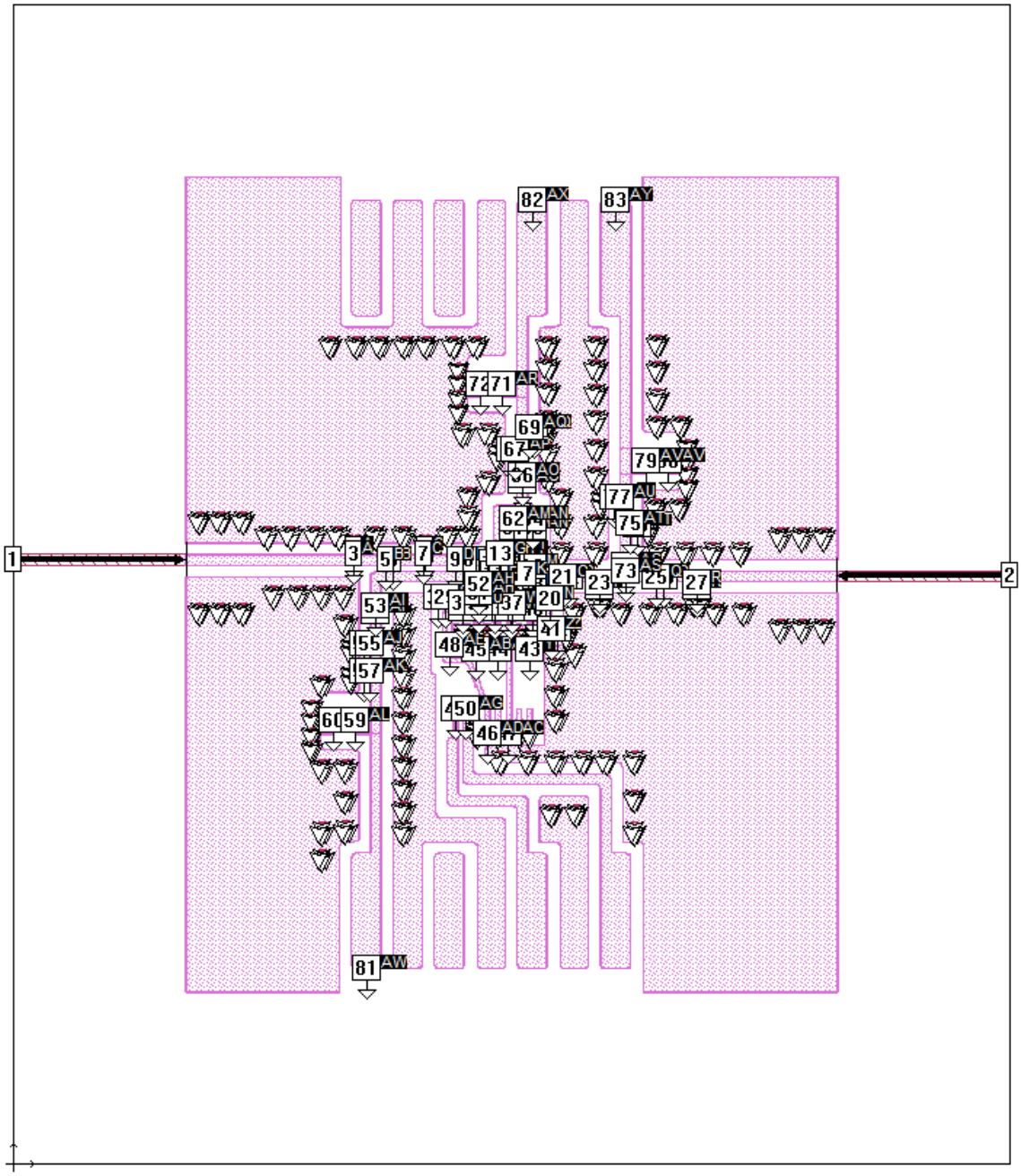


Figure H.1 TN_Prototype1 Layout on EM-Simulator

The layout of TN_Prototype1 was simulated in Sonnet™ full-wave simulator. The total number of ports used in the simulation was 83 ports (2 normal ports and 81 co-calibrated ports).

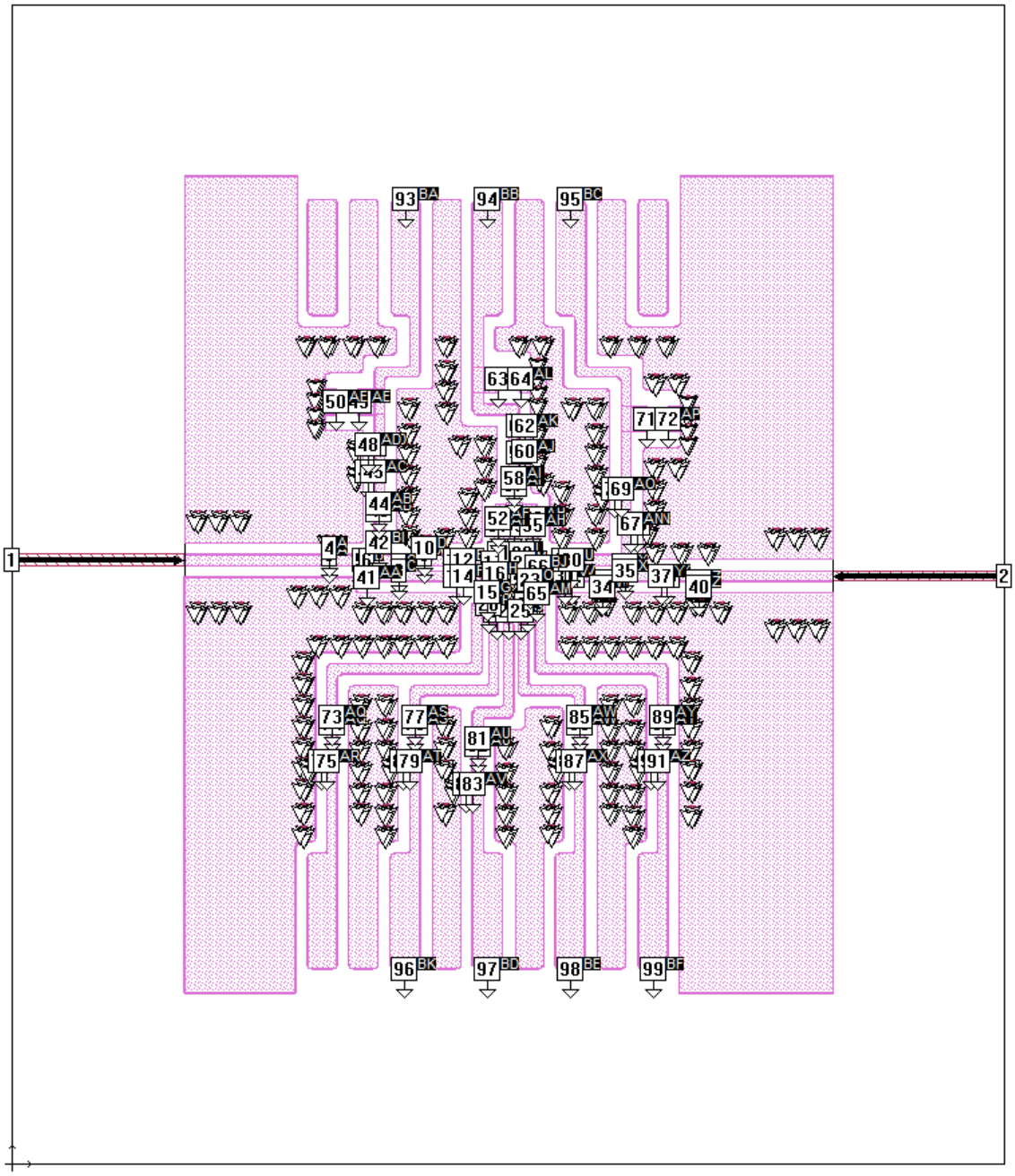
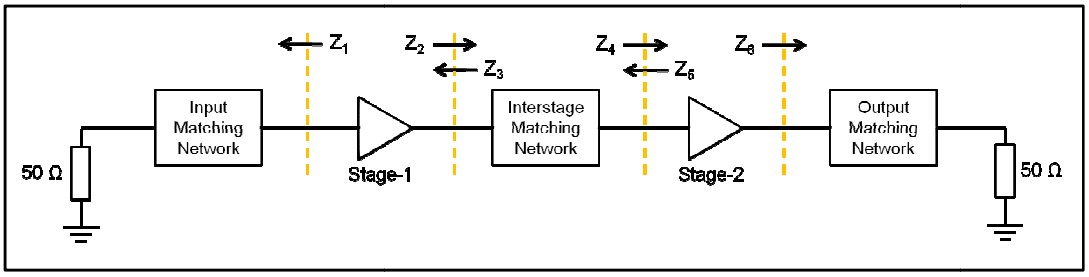


Figure H.2 TN_Prototype2 Layout on EM-Simulator

The layout of TN_Prototype2 was simulated in Sonnet^{TM} full-wave simulator. The total number of ports used in the simulation was 99 ports (2 normal ports and 97 co-calibrated ports).

APPENDIX I

INTERSTAGE IMPEDANCES



Interstage Impedances of DTN2

f_0	227 MHz	314 MHz	393 MHz	490 MHz	724 MHz
Z_1	51.663 – j3.910	51.671 – j2.833	51.681 – j1.655	51.693 – j0.466	51.708 – j0.807
Z_2	22.558 + j 4.729	22.796 + j 5.023	23.227 + j 5.478	23.898 + j 6.044	24.91 + j 6.675
Z_3	229.21 – j304.75	142.13 – j273.90	111.13 – j233.62	93.522 – j196.34	74.948 – j161.07
Z_4	17.313 + j10.259	18.594 + j1.567	15.908 + j1.581	10.250 + j3.029	7.441 + j2.946
Z_5	20.167 – j14.609	18.974 – j13.372	17.531 – j11.790	16.095 – j9.931	14.790 – j7.727
Z_6	51.015 + j10.228	51.613 + j7.846	51.935 + j5.225	51.865 + j2.628	51.295 – j0.020

Interstage Impedances of DTN3

f_0	217 MHz	314 MHz	383 MHz	441 MHz	763 MHz
Z_1	51.663 – j3.910	51.672 – j2.645	51.682 – j1.508	51.693 – j0.466	51.709 – j0.902
Z_2	22.558 + j 4.729	22.851 + j 5.086	23.296 + j 5.543	23.897 + j 6.044	25.006 + j 6.718
Z_3	218.30 – j208.48	163.61 – j184.26	116.98 – j143.38	97.094 – j97.80	80.964 – j56.028
Z_4	5.194 – j13.456	4.646 – j9.573	3.919 – j6.744	4.121 – j4.973	4.073 – j2.923
Z_5	20.167 – j14.609	18.750 – j13.137	17.348 – j11.574	16.095 – j9.931	14.706 – j7.557
Z_6	51.015 + j10.228	51.688 + j7.428	51.949 + j4.901	51.865 + j2.628	51.230 – j0.211

Interstage Impedances of TO0

f_0	1.37 GHz	1.60 GHz	1.71 GHz	1.95 GHz
Z_1	20.657 + j38.761	38.030 + j42.017	52.817 + j34.711	59.250 + j10.265
Z_2	24.560 – j15.610	20.949 – j10.834	20.349 – j7.355	20.438 – j5.594
Z_3	68.936 – j191.393	77.997 – j140.117	77.121 – j92.695	68.626 – j35.898
Z_4	41.584 – j50.639	26.421 – j52.935	17.237 – j48.664	11.492 – j41.468
Z_5	19.987 – j3.440	17.491 – j0.997	15.309 + j2.468	13.621 + j8.933
Z_6	15.133 + j0.399	14.196 + j4.686	15.509 + j9.150	26.117 + j7.888

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